

Design And FPGA-Based Implementation of An LTE-A/Non-Standalone 5G System With 1024-QAM

Sheeja Nair¹, Sunil Karamchandani²

¹Electronics and Telecommunication Engineering, Dwarkadas J. Sanghvi College of Engineering
University of Mumbai, India

shreeja.nair@djsce.ac.in

²Electronics and Telecommunication Engineering, Dwarkadas J. Sanghvi College of Engineering
University of Mumbai, India

sunil.karamchandani@djsce.ac.in

Abstract— This research investigates higher-order modulation schemes, such as 256-QAM and 1024-QAM, on the performance of LTE-Advanced (LTE-A) systems, aligned with the 3GPP evolution toward Non-Standalone (NSA) 5G architectures. By analyzing the performance of various modulation techniques, this work supports the downlink capacity improvements crucial for NSA 5G deployments where LTE-A serves as the control anchor. The system is modeled using MATLAB/SIMULINK and validated through real-time hardware testing on the MYIR Z-turn Zynq 7020 board. HDL code generation and implementation using Vivado and Vitis ensure a hardware-software co-design approach, showcasing system performance in near real-time conditions.

Keywords — LTE-A, fading channels, FPGA board, Zynq board, Vivado.

I. INTRODUCTION

The increasing demand for faster speeds, reduced latency, and more dependable connections is driving the rapid advancement of 5G mobile communication technology, which is changing wireless connectivity. LTE-A and 5G work together in various dynamic mobile contexts to deliver reliable, high-performance communication services. Advanced modulation techniques increase bits per symbol, optimize spectrum use, and improve overall throughput to increase data transmission efficiency [1]. With carrier aggregation and enhanced modulation capabilities, LTE-A is essential to the 5G transition because it allows current networks and cutting-edge technology to integrate seamlessly [2].

1.1 Objective

Based on the most recent 3GPP specifications, this paper investigates the usefulness of higher-order modulation in LTE-A and evaluates its effects on efficiency and performance. Even though 5G deployment is spreading worldwide, LTE-Advanced is still essential to contemporary communication networks. The study aims to improve spectral efficiency, guarantee signal dependability across various channel conditions, and tackle important implementation issues. It examines MIMO configurations and advanced modulation [3] schemes like 256QAM and 1024QAM to explore the performance collectively. This study examines transmitted bits and bit loss under different signal-to-noise ratio (SNR) conditions. To improve communication dependability, it looks more closely at the impacts of fading channels and suggests ways to lessen their influence. The paper uses MATLAB/SIMULINK simulations and hardware testing on the MYIR Z-turn Zynq 7020 platform to validate the findings [4].

1.2 3GPP Release

The Third Generation Partnership Project (3GPP), has dramatically improved LTE and sped up the transition to 5G, has been the driving force behind the advancement of mobile communications. While Release 13 focused on machine-type communications and public safety, Release 12 enhanced LTE to enable mission-critical services. Release 15 [5] marked the official launch of 5G with enhanced mobile broadband (eMBB), ultra-reliable low-

latency communications (URLLC), and massive machine-type communications (mMTC) capabilities. Release 16 has integrated enhanced performance and accommodates new applications. Release 17 [6] enhanced 5G with faster data speeds, massive connectivity, and more efficiency to support the growth of the Internet of Things and unlicensed spectrum. Release 18 [7] highlights faster data speeds, enhanced network efficiency, and improved connectivity, boosting overall performance. Key uses include augmented reality, smart manufacturing, and remote healthcare.

1.3 Research Route Map

The structure of the paper is as follows: Section II discusses technology in the communication system. Section III covers multiple access techniques, FPGA implementation using MATLAB/Simulink on the Zynq-7020 used for coverage is covered in Section IV. Followed by Section V discuss the result analysis with Section VI discuss the Conclusion.

II. ALAMOUTI CODING SCHEME FOR MIMO: ENCODER AND DECODER

Figure 1 shows 2x2 MIMO system utilizing Alamouti Space-Time Block Coding (STBC), two transmit antennas and two receive antennas are used to improve system reliability and combat fading [8]. The encoding process begins with two complex data symbols, s_1 and s_2 which are transmitted over two consecutive time slots. In Time Slot 1, the first transmit antenna (Tx1) sends symbol s_1 , while the second transmit antenna (Tx2) simultaneously transmits symbol s_2 . In Time Slot 2, the antennas transmit the conjugate and negated versions of the original symbols: Tx1 transmits $-s_2^*$ and Tx2 transmits s_1^* . This transmission strategy forms the Alamouti space-time block code, which can be mathematically represented by the following transmission matrix:

$$S = \begin{bmatrix} s_1 & -s_2^* \\ s_2 & s_1^* \end{bmatrix}$$

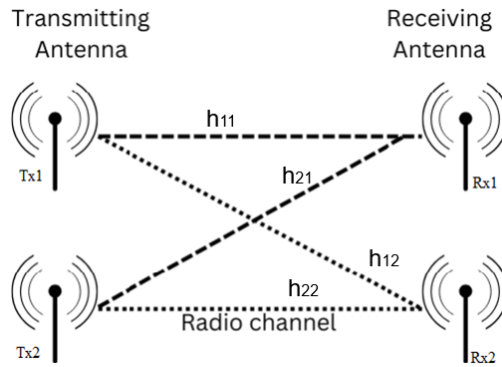


Figure 1. 2 x 2 MIMO [9]

The encoder ensures that both symbols s_1 and s_2 are transmitted from both antennas across two time slots, providing spatial and temporal diversity in the system. The channel gains from the transmit antenna i to receive Antennas j is h_{ij} along with $n_i(t_k)$ noise at Receive Antenna i at time slot t_k respectively. At Receiving Antenna 1 and 2 [10], during time slot t_1 , the received signal is :

$$r_1(t_1) = h_{11}s_1 + h_{21}s_2 + n_1(t_1) \quad (1)$$

$$r_2(t_1) = h_{12}s_1 + h_{22}s_2 + n_2(t_1) \quad (2)$$

At Receiving Antenna 1 and 2, during time slot t_2 , the received signal is:

$$r_1(t_2) = -h_{11}s_2^* + h_{21}s_1^* + n_1(t_2) \quad (3)$$

$$r_2(t_2) = -h_{12}s_2^* + h_{22}s_1^* + n_2(t_2) \quad (4)$$

To decode the transmitted symbols s_1 and s_2 , the receiver uses the known channel gains and combines the received signals from both antennas across two time slots. The idea is to exploit the orthogonality of the Alamouti code to separate and detect the transmitted symbols independently.

$$\bar{s}_1 = h_{11}^*r_1(t_1) + h_{21}r_1^*(t_2) + h_{12}^*r_2(t_1) + h_{22}r_2^*(t_2) \quad (5)$$

$$\bar{s}_2 = h_{21}^*r_1(t_1) - h_{11}r_1^*(t_2) + h_{22}^*r_2(t_1) - h_{12}r_2^*(t_2) \quad (6)$$

III. LTE-A: MULTIPLE ACCESS TECHNIQUES

Orthogonal Frequency Division Multiple Access (OFDMA) and Single Carrier Frequency Division Multiple Access (SC-FDMA) serve as the primary multiple access schemes for downlink and uplink channels, respectively [11]. SC-FDMA and OFDMA, adopted for uplink and downlink transmission [12] results in enhanced uplink data rates and spectral efficiency [13].

3.1 Transmitter and Receiver

The input data stream is transmitted at a rate of S symbols/second and is converted from serial to parallel using an S/P converter, transmitting limited bits per parallel line. The parallel data maps use M-QAM, such as 64-QAM, 256-QAM, and 1024-QAM. After modulation, the symbols undergo an M-point FFT, spreading the data across the subcarriers. The subcarrier-mapped symbols are then processed by an N-point IFFT, converting the frequency-domain symbols to the time-domain waveform [14]. A Cyclic Prefix (CP) is appended at the start of each symbol to combat Inter-Symbol Interference (ISI), increasing the length of the sample to $N + L_p$, where N is the number of subcarriers or FFT size, and L_p is the length of converted to serial format and transmitted through the channel. If $\{f_k, k \in 0, \dots, N-1\}$ are symbols to be transmitted, the OFDMA modulated signal is

$$s(t) = \sum_{m=-\infty}^{\infty} \sum_{k=0}^{N-1} f_k e^{j2\pi f_k t} p(t - mT) \quad (7)$$

The frequency of the k -th subcarrier, $f_k = f_0 + k\Delta f$, f_0 is the initial frequency of the first subcarrier, $\Delta f = 1/T$ Subchannel bandwidth, which ensures orthogonality between the subcarriers. The receiver reverses the transmitter's actions. The signal changes from a serial stream to parallel data at the receiver after demodulating and traveling over the fading channel. The time-domain samples undergo a transformation back to the frequency domain N-point Fast Fourier Transform (FFT) once the cyclic prefix (CP) has been eliminated.

3.2 Rayleigh and Rician

Rayleigh fading channel occurs in N-LOS. The amplitude of the received signal (r_0) and Variance of the fading amplitude (σ^2). Then, the PDF of Rayleigh channel [15] is

$$p(r_0) = \frac{r_0}{\sigma^2} \exp\left(-\frac{r_0^2}{2\sigma^2}\right) \text{ When } r_0 \geq 0 \quad (8)$$

Rician distribution describes the amplitude of a signal with a line-of-sight (LOS) component and multiple scattered paths. The probability density function (PDF) for Rician fading model [16] is given by:

$$p(r_0) = \frac{r_0}{\sigma^2} \exp\left(-\frac{r_0^2}{2\sigma^2}\right) \text{ When } r_0 \geq 0 \quad (9)$$

In general, the marginal distribution for the phase is dependent on θ and is obtained by integrating out R from the joint distribution:

$$f_\theta(\theta) = \frac{1}{2\pi} \exp\left(-\frac{s^2}{2\sigma^2}\right) + \frac{\tilde{m}}{2\pi\sigma} \exp\left(\frac{\tilde{m}^2 - s^2}{2\sigma^2}\right) Q\left(-\frac{\tilde{m}}{\sigma}\right) \quad (10)$$

3.3 Performance Metrics

The Symbol Error Rate (SER) for rectangular M-QAM can be derived by considering two orthogonal M-PAM signals on the In-phase (I) and quadrature-phase (Q) branches. The error probability of QAM [17] is obtained by analyzing the error probability of each branch, where Q is the Q-function representing the tail probability of the Gaussian distribution, $\bar{\gamma}_s$ is the average signal-to-noise ratio (SNR) per symbol, and M is the modulation order of the QAM constellation.

$$P_s = 1 - \left(1 - \frac{2(\text{sqrt} M - 1)}{\text{sqrt} M} Q\left(\sqrt{\frac{3\bar{\gamma}_s}{M-1}}\right)\right)^2 \quad (11)$$

IV. FPGA Implementation Using MATLAB/Simulink on Zynq 7020

LTE-A physical layer model is developed using MATLAB and Simulink, incorporating signal generation, QAM and OFDM modulation, cyclic prefix insertion, and channel modelling with Rayleigh and Rician fading. HDL Code Advisor and HDL Workflow Advisor verify the model's suitability for HDL generation. HDL Coder generates Verilog/VHDL code and a testbench for simulation and validation. The verified code is imported into Xilinx Vivado for RTL synthesis and timing analysis. The design is implemented on the MYIR Z-turn Zynq 7020 board, with PMOD LCD peripherals displaying real-time performance metrics like transmitted bits, BER, and bit loss.

4.1 MATLAB/SIMULINK

In MATLAB simulations of mobile communication systems, the standard setup usually comprises a transmitter, a Rayleigh fading channel, a receiver, BER analysis, and constellation diagram visualization. To reduce inter-symbol interference, a cyclic prefix is added. The Rayleigh fading channel models multipath fading, a typical scenario where signals reflect off different surfaces, leading to multiple delayed and attenuated versions of the signal arriving at the receiver. MATLAB's functions can mimic this by generating

random complex Gaussian variables to simulate the channel's impulse response. It proves powerful for channel estimation techniques. Its matrix operations support these methods, which are integral to mobile communication. These techniques aid in the development, simulation, and optimization of channel estimation algorithms in mobile communication. LS, MMSE, and LMS allow efficient adaptation to varying channel conditions, leading to improved signal quality and enhanced data retrieval. Accurate channel estimation mitigates distortions and interference, contributing to optimal signal quality and maximizing data retrieval from the source.

Channel Estimation in LTE, ref [18]

The Least-Squares (LS) channel estimator aims to minimize the overall sum of squared differences between the observed and estimated values. This objective is represented by the following formula:

$$\hat{h}_p^{LS} = (X_p^H X_p)^{-1} X_p^H Y_p \quad (12)$$

Where $\hat{h}_p^{LS}$ is the vector of estimated channel coefficients, X_p^H is the matrix of observed values (known input data) and Y_p is the vector of observed values (received signal). The purpose of LS estimation is to minimize the sum of the squared discrepancies between the estimated channel response and the received pilot symbols.

Application: It is frequently employed in OFDMA systems for channel estimate to achieve a precise depiction of the channel's response across various subcarriers.

The objective of the linear minimum mean square error (MMSE) channel estimator is to reduce the mean square error of the true parameter vector 'h' to the estimated parameter vector 'z'. The second-order statistics must be understood in detail. The LMMSE channel estimator performs better than the LS estimator but requires more computing power, as shown by the following expression

$$\hat{h}^{LMMSE} = R_{h,h_p} (R_{h_p,h_p} + \sigma_w^2 I)^{-1} \hat{h}_p^{LS} \quad (13)$$

where the $R(h_p, h_p)$ is the autocorrelation matrix at the pilot symbols point and $R(h, h_p)$ is the cross-correlation matrix between the channel and pilot symbol position, $\sigma_w^2 I$ is the noise variance in the system along with the identity matrix I .

Purpose: MMSE estimation considers the noise and interference in the communication channel, aiming to minimize the mean square error Between the estimated and true channel responses.

Application: MMSE is crucial for optimizing channel estimation in scenarios where noise and interference play significant roles, improving the accuracy of the estimated channel.

Table I: MATLAB/SIMULINK Release Notes, [19]

MATLAB/SIMULINK	Parameters
Supported OS	Windows, Mac OS, Linux
Version	2024a
Included Editions	Standard, Academic, Home, Student
Application Bitness	32bit, 64bit
Simulation Kernel	Yes

Table II: MATLAB/SIMULINK with Dynamic System Technologies [20]

Applications	Details
Control System	Design and simulate including PID and adaptive control
Signal Processing	Aids in developing and analyzing algorithms for audio, video, and communication systems
Communication System Design	Modulation, coding, and MIMO
Power System Simulation	Models and analyzes power systems, including grid stability and renewable energy integration
Robotics and Autonomous Systems	Supports simulating and testing robotic systems and autonomous vehicles

4.2 Xilinx Vitis

The Xilinx Vitis unified platform is specifically engineered to facilitate the creation and implementation of a diverse array of flexible systems, encompassing System-on-Chip (SoC) designs, Xilinx FPGAs, Alveo cards, cloud-based FPGAs, and embedded platforms. The research mostly centres around high-performance computing, embedded systems, and applications accelerated by field-programmable gate arrays (FPGAs). Vitis empowers developers to leverage several Xilinx hardware platforms for applications that require high-performance acceleration, making it a versatile tool for FPGA-based development. It allows for the utilisation of FPGA resources for activities that are normally handled by GPUs, by providing support for many programming languages and frameworks. Vitis AI is a specialised component of this platform designed exclusively for performing artificial intelligence (AI) inference tasks on Xilinx hardware. The platform provides a range of tools and libraries specifically designed to improve and expedite artificial intelligence jobs on Xilinx field-programmable gate arrays (FPGAs) and reconfigurable system-on-chips (SoCs).

AI Model: A collection of pre-trained machine learning and deep learning models.

AI Optimizer: Adjusts model parameters during training to minimize the loss function and enhance performance.

Table III: Xilinx Release Notes, [21]

Xilinx	Parameters
Supported OS	Windows, Linux
Version	2024.1
Included Editions	Vivado, Vitis, ISE
Application Bitness	64bit
Simulation Kernel	Yes

Table IV: Xilinx with FPGA-Based System Design Technologies [22]

Applications in FPGA-Based System Design	Details
High-Level Synthesis	Enables the development of hardware using high-level programming languages.
Hardware Acceleration	Provides tools for accelerating computational tasks using FPGA hardware.
Embedded System Design	Supports the design and implementation of embedded systems with customizable hardware.
High-Performance Computing	Facilitates the development of high-performance computing solutions using FPGAs.
Signal Processing	Provides tools for designing and implementing signal processing algorithms on FPGA hardware.

Simulink block diagrams calculate performance metrics such as BER and SNR optimized for HDL generation through fixed-point conversion. The HDL library in Simulink generates generic HDL code or IP cores for the Zynq 7020. The process includes HDL generation, linting, synthesis, and implementation to optimize resource usage. The final HDL code is deployed on the FPGA, ensuring the system meets design specifications.

V. RESULT ANALYSIS

The Simulink model in Figure 2 uses 1024-QAM modulation to transmit data through an SC-FDMA system and OFDMA at the receiver. It calculates the Bit Error Rate (BER) and Signal-to-Noise Ratio (SNR) by comparing the transmitted and received signals. The spectrum scope visualizes the transmitted signal, while error rate calculation helps evaluate system performance. Table 1 below exemplifies the Bit Error Rate (BER) performance for Signal-to-Noise Ratio (SNR).

$$BER = \frac{\text{No. of Error bits}}{\text{No. of Transmitted bits}}$$

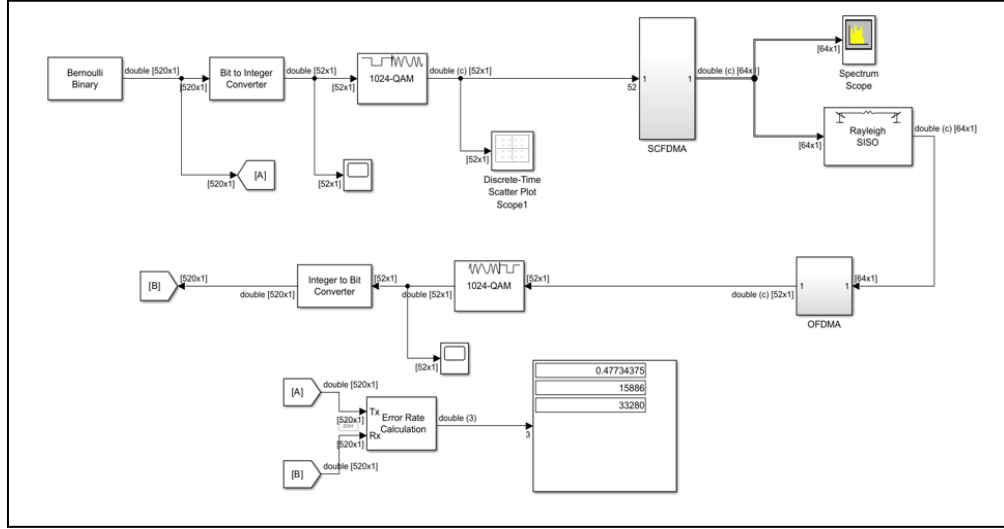


Figure 2. Rayleigh Channel with 1024 QAM Simulink Block

It is observed that, as SNR increases BER drops steadily. Among the schemes, 64-QAM shows the lowest BER at higher SNR values, demonstrating better noise resilience, whereas 1024-QAM maintains the highest data rates at the cost of increases BER, highlighting its sensitivity to noise.

Table V: Rayleigh Channel with different QAM

M SNR	64 QAM	256 QAM	1024 QAM
5db	0.474075	0.531374	0.541593
10db	0.415217	0.510447	0.536989
15db	0.370481	0.491814	0.530261
30db	0.281447	0.444697	0.515097
60db	0.190966	0.374771	0.488017
90db	0.144748	0.324506	0.464079

Table V measured the number of transmitted bits, bit loss, and packet loss for Rayleigh fading channels for 64-QAM, 256-QAM, and 1024-QAM modulation schemes. It is observed from the table that the modulation increases it increases the number of bits transmitted along with increase in the bit error loss. Table VI compares SISO and MIMO (2x1 and 2x2) configurations under a Rayleigh fading channel. The number of transmitted bits, bit error loss, and packet loss are compared for different layers.

Table VI: Rayleigh Channel with Alamouti Coding

Parameter	SISO	MIMO 2x2	MIMO 4x4
No. of Transmitted Bits	19656	39936	79872
No. of Error bits	9121	19325	39911
BER	0.4640	0.4878	0.4996

Figure.3 illustrates the Bit Error Rate (BER) versus Signal-to-Noise Ratio (SNR) performance of 64-QAM, 256-QAM, 1024-QAM upto 2048 QAM under nLOS channel. It is observed that as the SNR increases, the BER significantly decreases, demonstrating improved transmission reliability. Among the three, 64-QAM exhibits the lowest BER indicating better robustness to noise. In contrast, higher-order modulations like 256-QAM and 1024-QAM require higher SNR to achieve comparable BER performance due to their increased symbol complexity and denser constellation points.

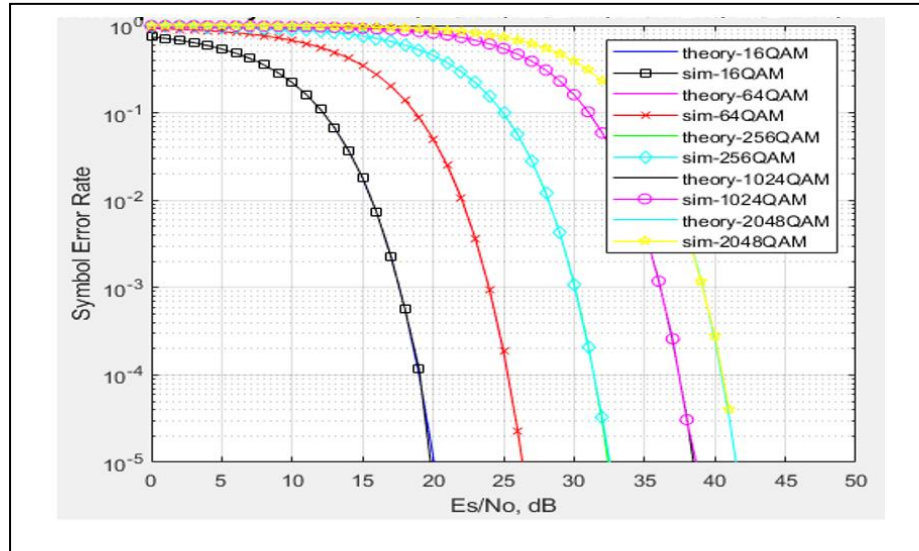


Figure.3 BER Versus SNR

The Simulink model shown in Figure.4 demonstrates a performance evaluation of SC-FDMA and OFDMA transmission schemes using a 1024-QAM modulation over a Rayleigh fading channel with integrated forward error correction (FEC) techniques. The system incorporates a convolutional encoder and a Viterbi decoder to enhance transmission reliability based on the proprietary 3GPP LTE-Advanced (LTE-A) standard. A Bernoulli binary generator initially creates random input data, which is then encoded using the convolutional encoder for error correction. The encoded bits are mapped to symbols using 1024-QAM modulation. The signal follows two paths: an SC-FDMA transmitter and Rayleigh SISO channel, and a standard OFDMA path. The SC-FDMA signal is demodulated at the receiver and passed through a Viterbi decoder for error correction.

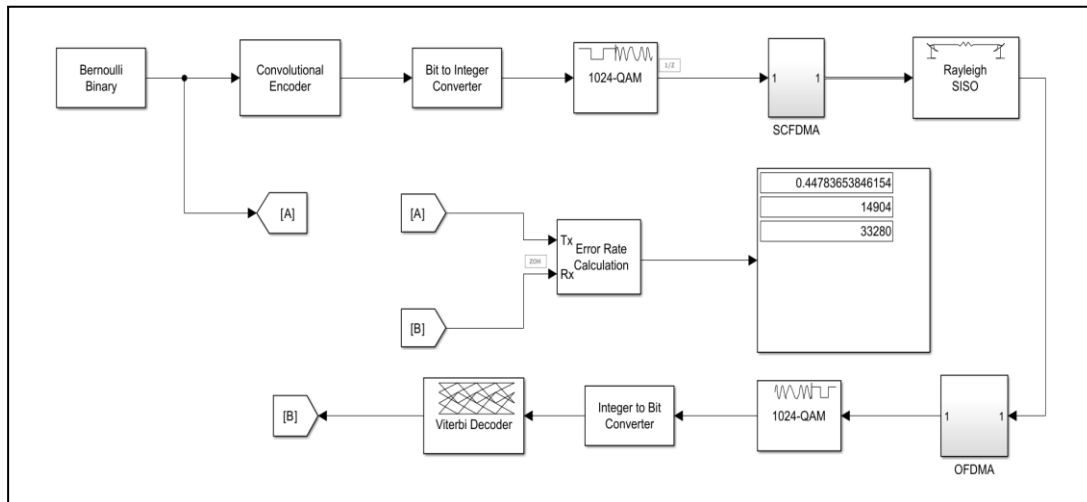


Figure.4 Error Detector1024 QAM Simulink Block

From Table V and VI it's observed that as the modulation and layers increase it also increases the bit losses. To reduce the bit error and increase the spectral efficiency error correction technique is used. Table VII provides a comparative analysis of 1024- QAM modulation with and without applying an error correction technique, explicitly using a convolutional encoder and Viterbi decoder. The system with error correction reduces overall losses. Consequently, the packet loss is reduced by improving the overall efficiency of the system.

Table VII: Error Correction Technique

Parameters	1024-QAM With Error Correction	1024-QAM Without Error Correction
No. of Transmitted Bits	33280	33280
Bit Loss	14904	15886
Packet Loss	0.44783	0.47734

Figure. 5 depicts HDL compatible fixed-point based Simulink model. Block design in Vivado, developed for Zynq-based system (MYIR Z-turn Zynq 7020 board). The design integrates a Processing System (PS) block connected to various Advanced Extensible Interfaces (AXI), including AXI Interconnect and AXI General-Purpose Input/Output (GPIO) modules.

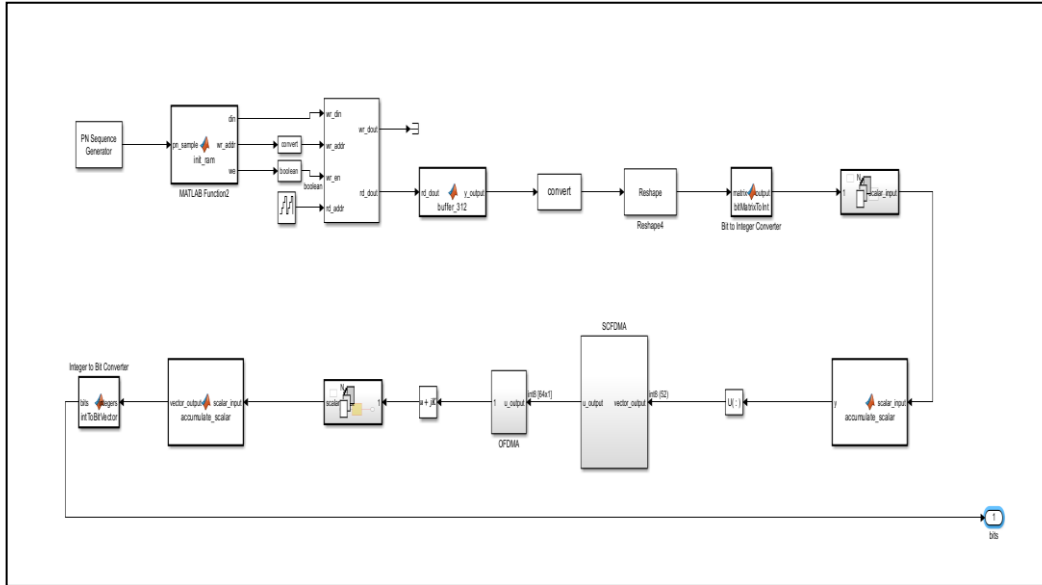


Figure.5 HDL Block Diagram in Vivado

IP cores such as AXI DMA (Direct Memory Access) and AXI peripherals communicate with the PS. A clocking wizard provides the necessary system clocks, while PMOD peripherals are connected to display performance metrics. The Subsystem_0 block suggests additional custom logic or hardware IP for handling data processing tasks.



Figure.6 FPGA Testbed

The design was built on the MYIR Zynq-7020 development board as shown in Figure 6. While Vitis was used for software development, including platform creation, application creation, compilation, and deployment, Vivado was used for hardware design, IP integration, RTL Analysis, Synthesis, Implementation and bitstream generation. The FPGA board is interfaced to the host computer via JTAG interface for programming and debugging. The Zynq-7020 SoC platform could run and validate the designated system in real time due to the smooth integration of the hardware and software component.

VI CONCLUSION

Evaluating SISO and MIMO configurations under AWGN and Rayleigh fading channels using 64-QAM, 256-QAM, and 1024-QAM modulation schemes reveal the inherent trade-offs between data rate and reliability. While higher-order modulations like 1024-QAM significantly boost throughput, they are more susceptible to noise and channel fading resulting in elevated bit and packet loss. To mitigate these impairments, a Viterbi decoder paired with a convolutional encoder is employed, effectively reducing errors and enhancing data integrity. This error correction mechanism proves particularly beneficial in sustaining the performance of 1024-QAM under degraded channel conditions. MIMO further improves robustness and signal quality, making it suitable for high-throughput wireless communication. These techniques are particularly applicable in LTE-Advanced (LTE-A) systems, which play a pivotal role in Non-Standalone (NSA) 5G deployments where LTE-A manages the control plane while 5G NR delivers enhanced data capabilities.

The RTL-level design and HDL block integration using Xilinx Vivado, followed by implementation on the MYIR Z-turn Zynq-7020 board, provides a comprehensive co-design platform. Leveraging the Zynq SoC's dual-core ARM Cortex-A9 processor and programmable logic fabric enables real-time data processing and hardware acceleration critical for validating LTE-A/NSA 5G protocols. The Vivado-generated synthesis layout supports performance evaluation and optimal resource allocation, ensuring scalability and reliability in dynamic wireless environments. This combined simulation-to-hardware validation workflow demonstrates the practical feasibility of deploying high-order modulation schemes like 1024-QAM in real-world 4G and 5G infrastructure, enhancing system capacity, user connectivity, and spectrum efficiency.

REFERENCES

- [1] Y. Yuan, L. Lina, H. Chen, Q. Huang, and J. Gong, "Resource allocation of 5G mmWave communication under random interference," *Scientific Reports*, vol. 15, no. 1, p. 9120, 2025.
- [2] S. Saleem and M. Lodro, "Resilience of LTE-A/5G-NR links against transient electromagnetic interference," *arXiv preprint arXiv:2501.11389*, 2025.
- [3] Singya, Praveen Kumar, Parvez Shaik, Nagendra Kumar, Vimal Bhatia, and Mohamed-Slim Alouini, "A survey on higher-order QAM constellations: Technical challenges, recent advances, and future trends," *IEEE Open Journal of the Communications Society* 2 (2021): 617-655.
- [4] C. Sudarshan, C. Chetan, A. Arora, and V. A. Chhabria, "GreenFPGA: Evaluating FPGAs as environmentally sustainable computing solutions," *Proceedings of the 61st ACM/IEEE Design Automation Conference*, pp. 1-6, 2024.
- [5] X. Lin et al., "5G from space: An overview of 3GPP nonterrestrial networks," *IEEE Communications Standards Magazine*, vol. 5, no. 4, pp. 147-153, December 2021.
- [6] A. Ghosh, A. Maeder, M. Baker, and D. Chandramouli, "5G evolution: A view on 5G cellular technology beyond 3GPP release 15," *IEEE access*, vol. 7, pp. 127639-127651, 2019.
- [7] X. Lin, "The bridge toward 6G: 5G-Advanced evolution in 3GPP Release 19," *IEEE Communications Standards Magazine*, vol. 9, no. 1, pp. 28-35, 2025.
- [8] Q. J. Kadhim, A. Al-Husseini, and M. Al-Ibadi, "Accuracy comparison of hard, soft, and unquantized decisions across diverse MIMO channels and M-QAM demodulation," *Technology*, vol. 6, no. 1, pp. 1-16, 2025.
- [9] Ali, Ahmed K., and Ergun Erçelebi, "An M-QAM Signal Modulation Recognition Algorithm in AWGN Channel," *Scientific Programming* 2019, no. 1 (2019): 6752694.

- [10] S. Qureshi, "Quadrature Amplitude Modulation (QAM)," Wireless Pi, [Online]. Available: <https://wirelesspi.com/quadrature-amplitude-modulation-qam/>. [Accessed: 18-Mar-2025].
- [11] MathWorks, "SC-FDMA vs. OFDM," MATLAB & Simulink, 2024. [Online]. Available: <https://in.mathworks.com/help/comm/ug/scfdma-vs-ofdm.html>. [Accessed: 19-Mar-2025].
- [12] Z. Augustine, H. Bello, A. M. S. Tekanyi, A. S. Yaro, H. A. Abdulkareem, O. O. Umeonwuka, and U.-F. Abdu-Aguye, "Generation of 5G frequency one model based on orthogonal multiple access technique of filtered-orthogonal frequency division multiplexing scheme for advanced interference evaluation," *Computers and Electrical Engineering*, vol. 123, p. 110056, 2025.
- [13] P. Tarafder, C. Chun, A. Ullah, Y. Kim, and W. Choi, "Channel estimation in 5G-and-beyond wireless communication: A comprehensive survey," *Electronics*, vol. 14, no. 4, p.750, 2025.
- [14] Mousavi, H., Iraj S. Amiri, M. A. Mostafavi, and C. Y. Choon, "LTE physical layer: Performance analysis and evaluation," *Applied computing and informatics* 15, no. 1 (2019): 34-44.
- [15] A. Abdelbari and B. Bilgehan, "The Derivation of The Probability of Error for BPSK, 16-QAM and 64-QAM in Rayleigh Fading Channel: A Unified Approach," *arXiv preprint arXiv:2406.16548*, 2024.
- [16] Simon, Marvin K., and Mohamed-Slim Alouini. "Digital communication over fading channels," *Digital Communication Techniques-Signal Design and Detection*. Englewood Cliffs, NJ: PTR Prentice-Hall (1995).
- [17] Assaf, Tasneem, Arafat Al-Dweik, Mohamed El Moursi, and Hatem Zeineldin, "Exact BER performance analysis for downlink NOMA systems over Nakagami-fading channels," *IEEE Access* 7 (2019): 134539-134555.
- [18] P. Chawla and B. Gupta, "BER analysis of single/multi-user LTE and LTE-A systems," in *2014 IEEE International Advance Computing Conference (IACC)*, 2014, pp. 262–266.
- [19] D.-N. Le, A. K. Pandey, S. Tadeipalli, P. S. Rathore, and J. M. Chatterjee, *Network modeling, simulation and analysis in MATLAB: theory and practices*. John Wiley & Sons, 2019.
- [20] Agarwal, A., & Mehta, S. N. (2016). Design and performance analysis of MIMO-OFDM system using different antenna configurations. *2016 International Conference on Electrical, Electronics, and Optimization Techniques (ICEEOT)*, 1373–1377.
- [21] M. Simko, D. Wu, C. Mehlführer, J. Eilert, and D. Liu, "Implementation aspects of channel estimation for 3GPP LTE terminals," in *17th European Wireless 2011-Sustainable Wireless Technologies*, 2011, pp. 1–5.
- [22] S. Mikkili, A. K. Panda, and J. Prattipati, 'Review of real-time simulator and the steps involved for implementation of a model from MATLAB/SIMULINK to real-time', *Journal of The Institution of Engineers (India): Series B*, vol. 96, pp. 179–196, 2015.