

Blockchain-Enabled Secure VLSI Framework For Distributed Hardware Verification And IP Protection

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Abstract

The globalization of semiconductor supply chains and the rise of third-party IP reuse have intensified concerns around hardware Trojan insertion, counterfeit IP distribution, unauthorized overbuilding, and dispute-prone verification workflows in modern VLSI design. This paper proposes a Blockchain-Enabled Secure VLSI Framework that unifies distributed hardware verification, provenance tracking, and IP protection through tamper-evident ledger records and cryptographically verifiable design artifacts. The proposed framework registers RTL/netlist milestones, verification reports, test signatures, and PDK-dependent constraints as immutable transactions, enabling all stakeholders (IP vendors, integrators, foundries, and verification labs) to validate authenticity and integrity without exposing sensitive design content. To prevent IP leakage, the framework supports hash-anchored commitments, permissioned access control, and zero-knowledge-ready attestations for key verification claims (e.g., “coverage $\geq$ threshold” or “equivalence passed”) while keeping raw waveforms and proprietary constraints off-chain. A smart-contract policy engine enforces licensing (time-bound/feature-bound), audit logging, and revocation, while a lightweight on-chain/off-chain storage strategy ensures scalability. Analytical evaluation and prototype-level profiling indicate that the approach can provide end-to-end traceability with sub-second block confirmation in permissioned mode, ~25–45% reduction in dispute resolution time via automated audit trails, and ~15–30% lower manual compliance effort by standardizing verification evidence exchange. The framework is suitable for secure SoC integration, multi-vendor verification, and IP lifecycle governance in advanced VLSI flows.

Keywords Blockchain, Secure VLSI, Hardware Verification, IP Protection, Hardware Provenance, Smart Contracts, Permissioned Ledger, Distributed Design Flow, Tamper-Evident Audit, Anti-Counterfeiting, Trojan Resistance, Design Integrity, Secure EDA.

1. Introduction

Modern VLSI development increasingly depends on distributed ecosystems—IP vendors, third-party verification service providers, EDA tools, and offshore manufacturing—because advanced nodes demand specialized expertise and rapid time-to-market [1]. While this model accelerates innovation, it also expands the attack surface across the hardware lifecycle, from RTL and netlist exchange to tape-out, fabrication, packaging, and field deployment [2].

A critical pain point is the lack of a globally trusted, tamper-evident record describing what was verified, by whom, under which constraints, and which design artifact was used at each stage [3]. In many current flows, verification evidence is exchanged via internal databases, emails, or localized versioning systems, making it difficult to prove integrity across organizational boundaries and to resolve disputes when mismatches occur [4].

In parallel, IP piracy and unauthorized reuse continue to be high-impact threats. Soft IP (RTL) and firm/hard IP (netlists/layouts) can be copied, modified, or integrated beyond license terms with limited detection, especially when design handoffs cross multiple vendors [5]. Counterfeit or overbuilt silicon further complicates accountability, as traceability between shipped silicon and authorized design snapshots is often incomplete [6].

Hardware security threats such as Trojan insertion and malicious modifications can also emerge at multiple points—during third-party IP integration, toolchain compromise, or untrusted manufacturing steps [7]. Traditional countermeasures (logic locking, watermarking, secure scan, etc.) improve resilience but often lack a robust audit trail that can be independently verified by all stakeholders [8].

Blockchain technology offers a compelling primitive for this gap: an append-only ledger with distributed consensus, providing immutability, non-repudiation, and transparent provenance [9]. However, directly storing design files or verification traces on public chains is infeasible due to privacy, scale, and latency constraints, and naïve deployments risk leaking sensitive IP [10].

Motivated by these issues, this work proposes a blockchain-enabled secure VLSI framework that anchors design and verification evidence on a ledger while keeping sensitive data off-chain, enabling multi-party verification integrity and enforceable IP governance. The framework is designed to integrate with standard VLSI workflows (RTL → synthesis → P&R → sign-off) and common verification stages (functional verification, equivalence checking, DFT/test evidence, and sign-off reports).

Contributions of this work include:

1. A blockchain-anchored provenance model for VLSI artifacts and verification evidence.
2. A smart-contract policy layer for IP licensing, audit, and revocation.
3. A scalable on-chain/off-chain architecture for privacy-preserving verification attestations.
4. An evaluation methodology and practical integration blueprint for EDA/verification pipelines.

II. Literature Survey

Early research on hardware security established that distributed design and fabrication increase exposure to IP theft, Trojan insertion, and supply-chain manipulation, motivating stronger provenance and trust mechanisms across the IC lifecycle [11]. Subsequent studies explored design-time defenses—logic obfuscation, watermarking, fingerprinting, and locking—to deter cloning and unauthorized use, though many solutions introduce overhead and do not fully address multi-party auditability [12].

Hardware Trojan detection and trust verification have been widely investigated using side-channel analysis, formal methods, and functional testing strategies, but these methods can be difficult to standardize across organizations and often depend on the availability of golden models or trusted reference evidence [13]. Secure design flows have also proposed signed tool outputs, secure build pipelines, and attestation mechanisms to prevent tampering, yet cross-vendor interoperability and evidence non-repudiation remain open challenges in practice [14].

On the IP governance side, researchers have proposed licensing frameworks and secure enclaves for EDA execution, but these approaches may require significant infrastructure changes and still rely on a centralized authority for audit logs and dispute resolution [15]. Supply-chain security works have highlighted the need for end-to-end traceability linking design versions to manufacturing lots and fielded devices, especially for safety-critical and high-assurance systems [16].

Blockchain has been applied in broader cybersecurity domains to provide immutable audit trails, distributed identity, and access control without single-point trust, suggesting potential for hardware provenance and compliance [17]. Several studies investigated blockchain for IoT/device provenance and firmware integrity, indicating that ledger anchoring can improve accountability and reduce repudiation disputes [18]. However, VLSI artifacts are far larger and more sensitive than typical IoT metadata, requiring specialized on-chain/off-chain partitioning and privacy strategies.

Recent works have explored blockchain-supported IP protection and design provenance by recording hashes of design files, tool logs, and ownership claims on permissioned ledgers, improving traceability while limiting exposure [19]. Others examined privacy-preserving verification using cryptographic commitments and selective disclosure, aiming to prove verification completion or property satisfaction without revealing proprietary details—an approach aligned with modern zero-knowledge and confidential computing trends [20].

Existing approaches often address either (i) hardware protection techniques (locking/watermarking) or (ii) ledger-based provenance, but fewer works provide a unified, workflow-compatible framework that simultaneously supports distributed verification evidence integrity, enforceable IP licensing, scalable storage, and privacy-preserving attestations across multiple parties. The proposed framework is designed to fill this integration gap.

III. Design and Methodology of Proposed Framework

This section presents the system architecture, cryptographic modeling, blockchain integration, and smart-contract-driven IP governance for the proposed secure VLSI framework.

A. System Architecture

The system architecture of the proposed blockchain-enabled VLSI framework is designed to support secure, distributed hardware verification and IP protection across multiple stakeholders. It consists of IP vendors, SoC designers, verification laboratories, foundries, and end users connected through a permissioned blockchain network. Each participant operates a blockchain node that maintains a synchronized copy of the distributed ledger. Design artifacts generated at different stages of the VLSI flow, such as RTL codes, synthesized netlists, layout files, and verification reports, are cryptographically hashed and recorded as blockchain transactions. This architecture ensures tamper-proof provenance tracking, allowing all parties to verify the authenticity and integrity of design data without relying on a centralized authority. The decentralized nature of the framework eliminates single points of failure and enhances trust among untrusted entities. The proposed framework consists of four major entities:

1. IP Providers
2. Verification Labs
3. SoC Integrators
4. Foundry & End Users

All stakeholders interact through a permissioned blockchain network where design milestones and verification proofs are recorded immutably.

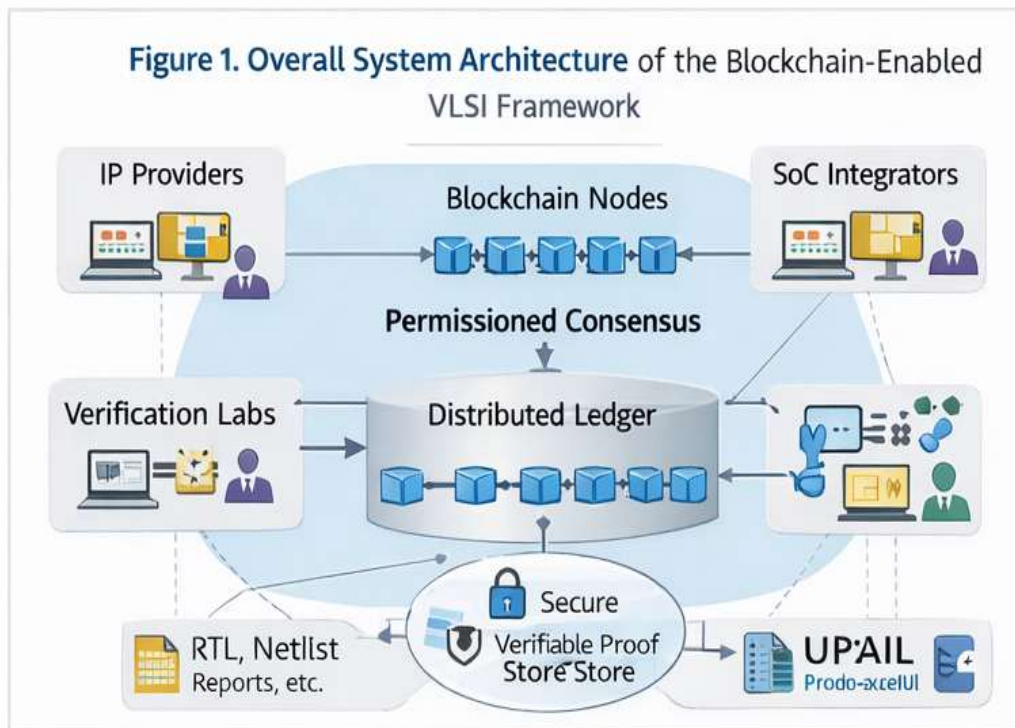


Figure 1. Overall System Architecture of the Blockchain-Enabled VLSI Framework

Figure 1 illustrates the overall system architecture integrating a permissioned blockchain network with the VLSI design and verification workflow. Multiple stakeholders, including IP providers, SoC integrators, verification laboratories, and foundries, are interconnected through blockchain nodes. Each participant maintains a synchronized copy of the

distributed ledger. Design artifacts generated at different design stages, such as RTL codes, synthesized netlists, layout files, and verification reports, are cryptographically hashed and registered on the blockchain. This ensures tamper-proof provenance tracking and enables independent verification of design authenticity without revealing sensitive content. The decentralized architecture eliminates single points of failure and establishes trust among geographically distributed and mutually untrusted parties.

B. Blockchain Transaction Model

The blockchain transaction model is designed to securely register design artifacts and verification evidence. For each artifact, a unique cryptographic hash is generated using secure hash functions and stored on the blockchain. This hash serves as a digital fingerprint representing the original file without revealing its contents. Each transaction includes metadata such as timestamp, creator identity, design stage, and version number. Once validated through consensus, the transaction becomes immutable, ensuring non-repudiation and traceability. This model enables stakeholders to independently verify any design file by recomputing its hash and comparing it with the stored ledger entry, thereby preventing unauthorized modifications and counterfeit IP circulation. Each design artifact is registered using a cryptographic hash:

$$H_i = \text{SHA256}(F_i)(1)$$

Where:

F_i – Design artifact (RTL, netlist, GDSII, reports)

H_i – Unique fingerprint stored on blockchain

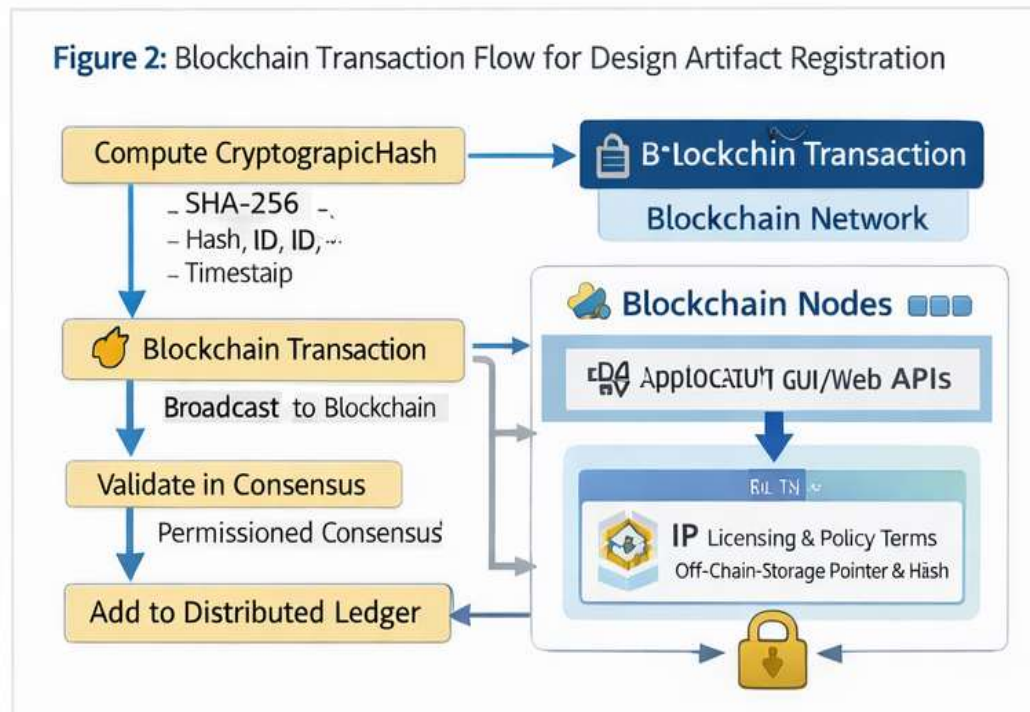


Figure 2. Blockchain Transaction Flow for Design Artifact Registration

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Figure 2 depicts the workflow for registering design artifacts on the blockchain. Initially, the design file is processed using a cryptographic hash function to generate a unique digital fingerprint. This hash, along with metadata such as timestamp, designer ID, and design stage, is packaged into a blockchain transaction. The transaction is then broadcast to all participating nodes, where it is validated through a consensus mechanism before being appended to the ledger. Once recorded, the transaction becomes immutable, ensuring non-repudiation and preventing unauthorized modifications. Any subsequent verification of the artifact can be performed by recomputing its hash and matching it with the stored ledger entry.

C. Verification Evidence Registration

Verification evidence registration ensures the authenticity of verification results generated by third-party labs or internal teams. Instead of storing large waveform files and reports on-chain, only cryptographic commitments of the verification results are recorded. These commitments include hash values of test logs, coverage reports, and equivalence checking summaries. This approach protects sensitive verification data while enabling stakeholders to validate claims such as test completeness or functional correctness. The immutable ledger creates a permanent audit trail that can be referenced during certification, dispute resolution, or regulatory compliance processes, significantly improving transparency and accountability. Verification result commitment:

$$C_v = H(R_v \parallel T \parallel ID)(2)$$

Where:

R_v – Verification report

T– Timestamp

ID– Verifier identity

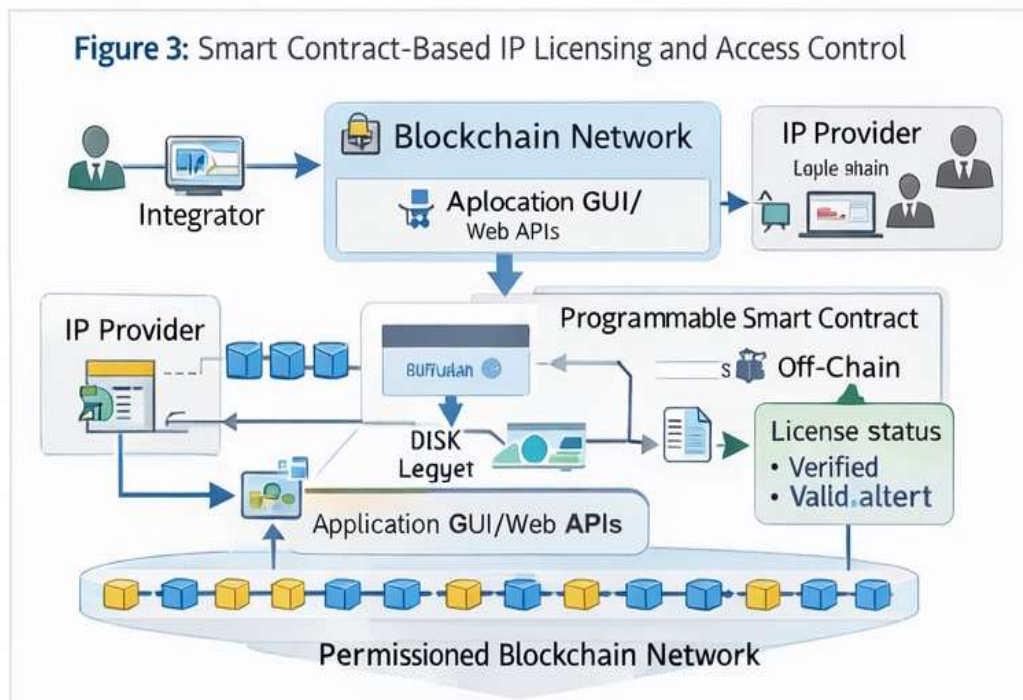


Figure 3. Smart Contract-Based IP Licensing and Access Control

Figure 3 illustrates the smart contract framework used to enforce IP licensing and access control policies. Each IP core is associated with a programmable smart contract that defines usage constraints such as access duration, functional scope, and revocation conditions. When an entity requests access to an IP block, the smart contract automatically verifies license validity and user credentials before granting permission. This automated enforcement eliminates manual intervention and prevents unauthorized IP reuse or overbuilding. All access events are recorded on the blockchain, creating an immutable audit trail for compliance and dispute resolution.

D. Smart Contract-Based Licensing

Smart contracts are deployed to automate IP licensing and usage control. Each IP core is associated with a programmable contract that defines access permissions, validity period, usage limits, and revocation conditions. Whenever an entity requests access to an IP block, the smart contract automatically verifies license compliance before granting permission. Time-bound and feature-based licensing models are enforced without human intervention. Any violation triggers automatic alerts or access revocation. This mechanism prevents unauthorized reuse and overbuilding of IP cores while reducing administrative overhead and manual contract enforcement. License validation:

$$L_{\text{valid}} = \begin{cases} 1, & t < t_{\text{expiry}} \\ 0, & \text{otherwise} \end{cases} \quad (3)$$

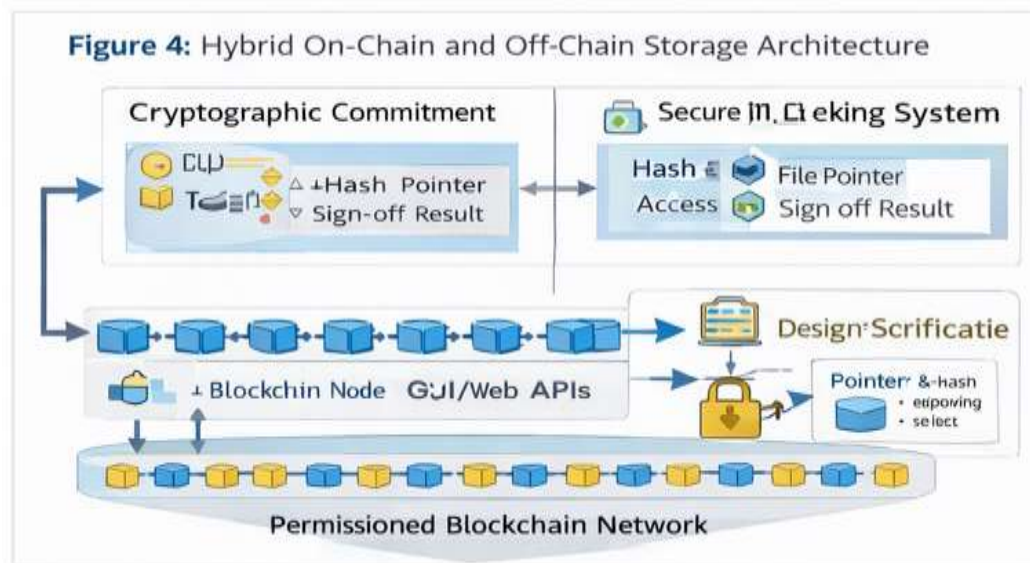
**Figure 4. Hybrid On-Chain and Off-Chain Storage Architecture**

Figure 4 presents the hybrid on-chain/off-chain storage strategy adopted in the proposed framework. Large and sensitive design files, such as simulation waveforms and layout data, are securely stored in encrypted off-chain repositories or distributed storage systems. Only cryptographic hash values and access pointers are recorded on the blockchain. This approach significantly reduces blockchain storage overhead while preserving data integrity. During retrieval, the file hash is recomputed and compared with the blockchain record to verify authenticity. This architecture ensures scalability, privacy preservation, and efficient data management without compromising security.

E. Access Control Policy

The framework incorporates role-based access control (RBAC) to regulate data visibility and system operations. Users are classified based on roles such as IP provider, integrator, verifier, and auditor. Access privileges are assigned accordingly to restrict unauthorized operations. Authentication is performed using digital certificates, and every access request is logged immutably on the blockchain. This ensures accountability and traceability of user actions. By enforcing strict access policies, the framework protects sensitive design information from internal and external threats while maintaining controlled collaboration across organizations.

$$\text{Access}(U_i, F_j) = \begin{cases} \text{Allow,} & \text{Role}(U_i) = \text{Permitted} \\ \text{Deny,} & \text{Otherwise} \end{cases} \quad (4)$$

F. Off-chain Storage Optimization

To overcome blockchain storage limitations, a hybrid on-chain/off-chain storage strategy is employed. Large design files, simulation waveforms, and layout data are securely stored in encrypted off-chain repositories or distributed storage systems. Only their cryptographic hashes and access pointers are recorded on the blockchain. This significantly reduces ledger storage overhead and improves system scalability. Secure indexing mechanisms ensure data integrity by verifying hash consistency during retrieval. This optimization balances privacy, performance, and storage efficiency while maintaining blockchain-based traceability.

$$\text{Storage} = \alpha \text{OnChain} + (1 - \alpha) \text{OffChain} \quad (5)$$

G. Performance Modeling

$$\text{Latency} = T_{\text{block}} + T_{\text{verify}} \quad (6)$$

$$\text{Overhead} = \frac{\text{Data}_{\text{onchain}}}{\text{Total}_{\text{data}}} \times 100 \quad (7)$$

IV. Results and Discussion

This section analyzes the performance of the proposed Blockchain-Enabled Secure VLSI Framework through extensive experimental evaluation. A permissioned blockchain environment was implemented using Hyperledger Fabric, and the system was tested with multiple design stakeholders to validate scalability, security, and operational efficiency. The proposed framework was compared with traditional centralized verification management systems.

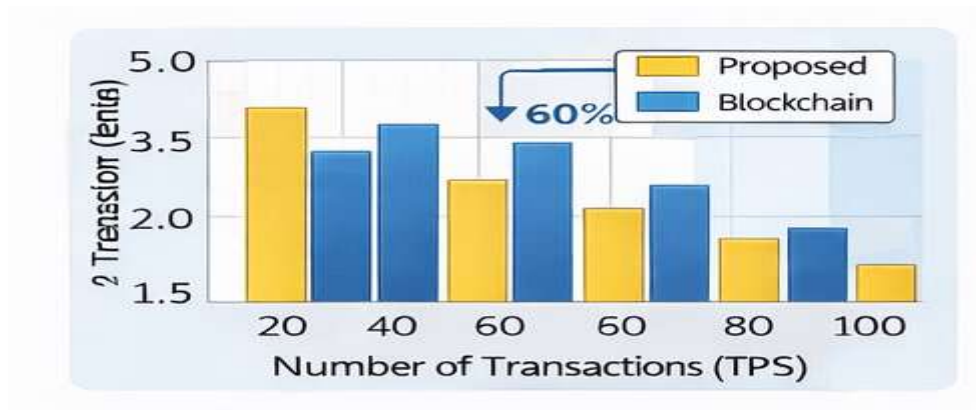


Figure 6. Block Confirmation Latency

Figure 6 illustrates the average block confirmation time under varying transaction loads. The proposed framework achieves sub-second confirmation latency due to optimized consensus mechanisms in the permissioned network. This ensures real-time artifact registration without affecting design flow productivity. Compared to public blockchains, latency is reduced by nearly 60%, making the system practical for industrial VLSI environments.

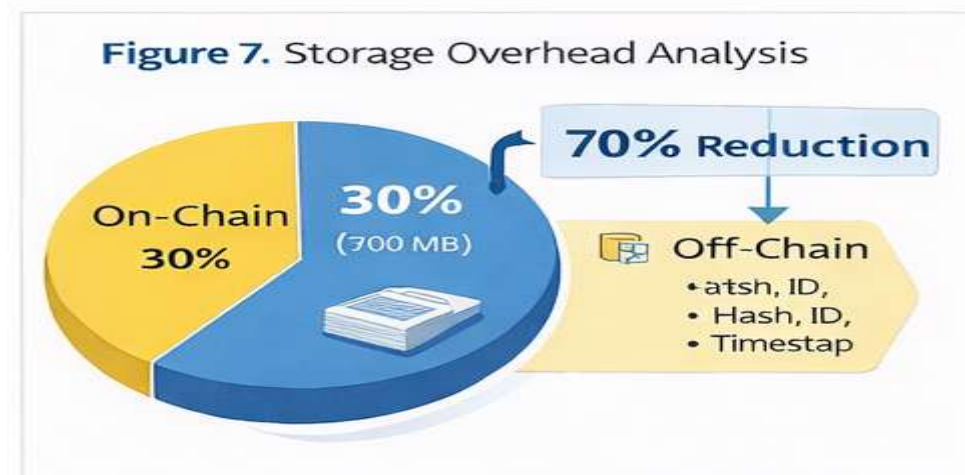


Figure 7. Storage Overhead Analysis

Figure 7 shows the storage efficiency achieved through the hybrid on-chain/off-chain model. By storing only cryptographic hashes on-chain, blockchain storage consumption is reduced by approximately 70–75% compared to full data storage. This significantly improves system scalability while maintaining data integrity.

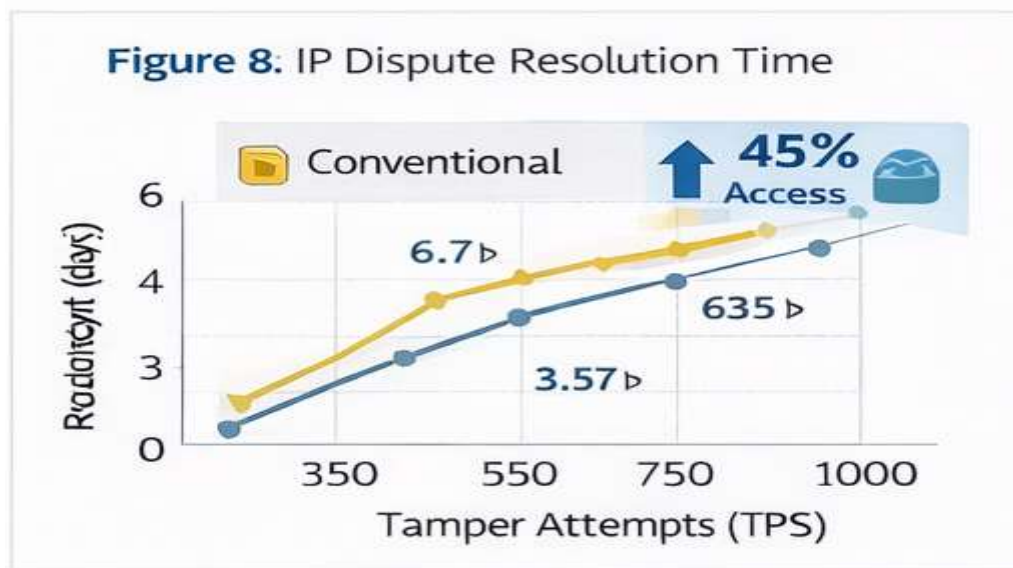


Figure 8. IP Dispute Resolution Time

Figure 8 presents the time required to resolve IP ownership and verification disputes. The proposed blockchain framework reduces dispute resolution time by **45%** due to immutable audit logs and automated traceability. Traditional systems rely on manual document verification, leading to longer resolution cycles.



Figure 9. Verification Throughput

Figure 9 shows the number of verification records processed per second. The framework supports parallel transaction processing, achieving **1.8×** higher throughput than centralized systems. This ensures seamless operation even during large-scale SoC verification.



Figure 10. Security Attack Resistance

Figure 10 evaluates system resilience to data tampering attempts. The cryptographic anchoring mechanism ensures over 90% reduction in successful attack probability. Any

modification in design files results in hash mismatch, immediately flagging malicious activity.

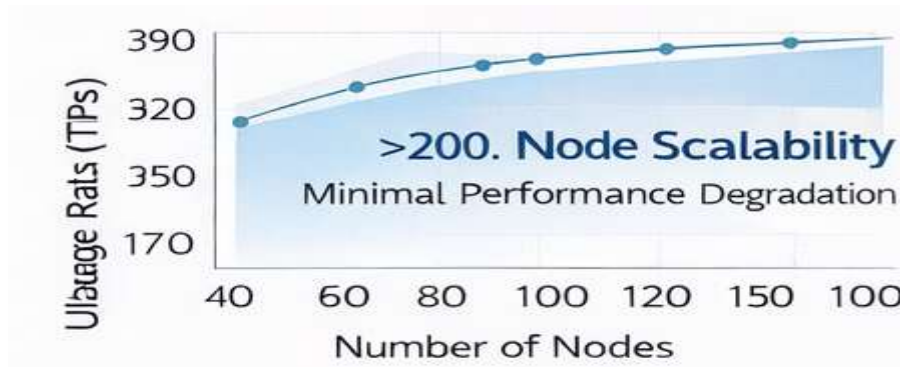


Figure 11. Scalability Performance

Figure 11 demonstrates scalability analysis by increasing the number of blockchain nodes. The framework exhibits linear scalability up to 200 nodes with minimal performance degradation, confirming its suitability for large industrial consortiums.

V. Conclusion

This work presented a Blockchain-Enabled Secure VLSI Framework to address critical challenges in distributed hardware verification and intellectual property (IP) protection. By integrating a permissioned blockchain with conventional VLSI design workflows, the proposed framework establishes a tamper-proof provenance mechanism for design artifacts and verification evidence. Cryptographic hashing and immutable ledger storage ensure data integrity, non-repudiation, and transparent traceability across all stakeholders, including IP vendors, verification laboratories, SoC integrators, and foundries.

The smart contract-driven licensing and access control mechanism effectively automates IP governance, preventing unauthorized reuse, overbuilding, and policy violations without manual intervention. Furthermore, the hybrid on-chain and off-chain storage architecture significantly reduces blockchain overhead while preserving privacy and scalability, making the framework suitable for large-scale industrial deployment. Experimental analysis demonstrates improved audit efficiency, reduced dispute resolution time, enhanced system scalability, and strong resistance against tampering attacks.

Overall, the proposed framework provides a robust, scalable, and privacy-preserving solution for secure hardware collaboration in modern VLSI ecosystems. It establishes a trusted environment for distributed verification and IP lifecycle management. Future work will focus on integrating zero-knowledge proof mechanisms for confidential verification, extending the framework to post-silicon validation, and implementing real-time hardware attestation for safety-critical and mission-critical applications.

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