

Cross-Technology Evaluation of a Gate-Diffusion-Input Magnitude Comparator for Scalable CMOS Architectures

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Abstract:

As modern digital systems demand enhanced computational efficiency under stringent power and area constraints, comparator circuits play a critical role in arithmetic and decision-making units. This paper presents a comprehensive cross-technology analysis of a Gate Diffusion Input (GDI)-based magnitude comparator implemented across multiple nanometer CMOS process nodes (180 nm, 90 nm, 45 nm, and 22 nm). The proposed design leverages the GDI technique to minimize transistor count, reduce static power dissipation, and improve switching performance compared to conventional CMOS and pass transistor logic structures. The comparator's structural optimization focuses on reducing logic redundancy while maintaining full-swing operation and high noise immunity. Simulation studies were conducted using Cadence Virtuoso and Tanner EDA tools, employing BSIM4 technology models for accurate device-level characterization. Key performance parameters—including propagation delay, power consumption, power-delay product (PDP), and area utilization—were evaluated and compared across technology nodes. Results indicate that the proposed GDI-based design achieves a 47.3% reduction in average power, 38.6% improvement in speed, and 52.1% lower PDP compared to traditional CMOS comparators in 22 nm technology. Moreover, the design demonstrates strong scalability and energy efficiency, making it suitable for integration into low-power VLSI systems, signal processing units, and embedded architectures. This cross-node analysis establishes GDI logic as a viable alternative for high-performance, power-efficient comparator design in emerging nanoscale technologies.

Keywords:

Gate Diffusion Input (GDI); magnitude comparator; CMOS scaling; low-power VLSI; nanometer technology; propagation delay; power-delay product (PDP); circuit optimization; energy-efficient digital design; Tanner EDA simulation.

Introduction

Gate-Diffusion-Input (GDI) logic has emerged as an influential low-power design paradigm, offering significant reductions in transistor count and switching activity compared to classical CMOS logic styles [1]. Magnitude comparators, which form the backbone of arithmetic and control subsystems in embedded processors, digital signal processors, and memory addressing units, greatly benefit from such power-aware logic optimizations [2]. As technology scaling continues into deep sub-micron and nanometer

nodes, maintaining performance while minimizing energy and area consumption has become increasingly challenging, prompting researchers to explore alternative logic styles capable of delivering superior efficiency [3].

The conventional CMOS-based magnitude comparator architecture, although robust and widely adopted, suffers from intrinsic limitations, particularly high dynamic power consumption arising from the need to charge and discharge internal capacitances at each switching event [4]. These challenges worsen in scaled technologies where leakage currents and process variations significantly impact circuit stability and reliability [5]. GDI offers an attractive solution by enabling logic implementation with fewer transistors and flexible input configurations that reduce power and delay [6].

However, the suitability of GDI circuits across diverse CMOS process technologies—such as 180 nm, 90 nm, 65 nm, and 45 nm nodes—remains a subject of active research due to the presence of threshold voltage variations, degraded noise margins, and body-biasing limitations [7]. Cross-technology evaluation is thus essential to understand whether GDI-based magnitude comparators maintain their advantages consistently when migrated across technology generations [8]. A comprehensive comparison must include performance metrics such as propagation delay, power dissipation, Power-Delay Product (PDP), and silicon area efficiency [9].

In high-performance and energy-constrained systems like IoT devices, biomedical implants, and unmanned aerial vehicles (UAVs), low-power comparators play a crucial role in enabling real-time decision making without exhausting battery resources [10]. As these applications increasingly adopt heterogeneous CMOS platforms ranging from traditional bulk CMOS to Fully-Depleted Silicon-On-Insulator (FD-SOI) and FinFET structures, cross-technology validation of logic architectures has become a necessity for design portability and scalability [11]. GDI's promise of reduced leakage and dynamic power must therefore be validated outside idealized simulation conditions.

Another key motivation for investigating cross-technology performance stems from the rapid transition from planar MOSFETs to multi-gate devices in commercial semiconductor manufacturing [12]. Although GDI logic provides superior energy efficiency in planar CMOS, its behavior in FinFET-based nodes, where body terminals are not independently accessible, raises concerns about functional correctness and design compatibility [13]. Understanding these trade-offs allows designers to adapt or hybridize GDI architectures for next-generation nanoscale systems.

Magnitude comparators themselves are prime candidates for such studies because they are ubiquitous in arithmetic units, sorting circuits, address decoders, digital filters, and cryptographic engines [14]. Small improvements in comparator delay or energy consumption often translate into significant system-level enhancements due to their high usage frequency inside control paths. Hence, analyzing the evolution of a GDI-based comparator across multiple semiconductor nodes provides insight into sustainable low-power hardware design practices.

Furthermore, the variability of GDI cell behavior under different supply voltages, threshold voltages, and environmental conditions necessitates robust modeling and simulation frameworks [15]. Deep technology scaling introduces stochastic phenomena such as Random Dopant Fluctuation (RDF), Line Edge Roughness (LER), and Bias Temperature Instability (BTI), which can degrade logic functionality. Cross-technology

evaluation therefore offers an opportunity to quantify the resilience of GDI-based designs under realistic fabrication conditions.

The increasing integration density of modern System-on-Chip (SoC) platforms also emphasizes the importance of area-efficient comparator implementations. GDI logic, with its inherent reduction in transistor count, contributes to smaller footprint designs that can directly impact chip yield and cost. Testing the architectural portability of such designs across technology nodes validates their long-term relevance for commercial VLSI design.

In addition, emerging applications such as machine learning accelerators, neuromorphic processors, and energy-aware edge-AI architectures demand ultralow-power circuit primitives capable of sustained operation under energy-harvesting or battery-restricted conditions. GDI-based comparators that consistently exhibit reduced PDP across nodes are better suited for these domains, making cross-technology evaluation a strategic requirement for next-generation circuit design.

Finally, as the industry moves toward heterogeneous integration, chiplet-based packaging, and 3D ICs, the ability to reuse optimized circuit components across diverse fabric technologies becomes essential. A systematic cross-technology evaluation of a GDI-based magnitude comparator not only highlights its strengths and weaknesses but also guides the development of scalable, fabrication-agnostic design methodologies for the semiconductor ecosystem. This study thus contributes to bridging the gap between device-level innovations and real-world system design requirements.

Literature Survey

Gate-Diffusion-Input (GDI) logic has received extensive attention in the low-power VLSI research community because of its capability to implement complex logic functions using significantly fewer transistors than conventional CMOS gates [16]. Early investigations demonstrated that GDI-based circuits offer reduced dynamic power consumption and enhanced operational speed due to minimized internal node capacitances, positioning GDI as a strong contender for ultra-low-power digital systems. These foundational insights triggered broader adoption of GDI logic in arithmetic and control circuits.

Magnitude comparators, widely used in ALUs, DSPs, memory addressing mechanisms, and cryptographic architectures, have undergone numerous design enhancements to improve power efficiency and computational delay [17]. Researchers have explored pass-transistor logic, dynamic logic, transmission gate logic, and hybrid CMOS techniques to reduce device count and switching activity. However, these methods often compromise noise margins or require multi-threshold devices, making them less suitable for scaled CMOS nodes.

The introduction of GDI-based comparators resolved several of these limitations by offering compact structures with reduced transistor overhead [18]. Studies consistently reported 30–60% reductions in area and power compared to classical CMOS designs. Nevertheless, these findings were primarily derived from single-technology simulations (e.g., 180 nm or 90 nm nodes), leaving questions about performance portability unanswered as device scaling continues.

Parallel to GDI development, extensive research investigated technology scaling trends and their implications on circuit reliability. Deep sub-micron processes introduce

increased leakage currents, random variations, and short-channel effects that significantly alter logic cell behavior [19]. Evaluating comparator architectures across nodes such as 130 nm, 65 nm, and 45 nm revealed nonlinear changes in delay and leakage, emphasizing the need for cross-technology evaluation frameworks.

Researchers in the FinFET and FD-SOI communities have further highlighted the importance of architecture adaptability, noting that body-biased or substrate-driven logic styles may not translate directly to multi-gate transistor technologies [20]. Since GDI relies heavily on source/body configuration flexibility, its adaptation to FinFET-based designs presents empirical challenges that require systematic investigation, especially for comparators that must maintain functional correctness under all bit conditions.

Numerous works have introduced optimized CMOS comparators using transmission gates, dynamic XOR cells, or high-speed precomputation units to reduce worst-case delay. Although these designs demonstrate superior performance in larger technology nodes, their scalability is constrained due to increased susceptibility to leakage and process variations in modern nodes [21]. This strengthens the relevance of exploring alternative logic families such as GDI for next-generation comparator designs.

Another significant research direction focuses on low-voltage operation, where maintaining correct logic levels becomes challenging due to threshold voltage shifts and degraded noise margins. GDI logic has shown promising performance under reduced supply voltages because of its compact structure and low switching activity [22]. However, comparative studies across process technologies remain limited.

Several studies also examined hybrid logic approaches that blend CMOS, PTL (Pass Transistor Logic), and GDI principles to mitigate disadvantages associated with individual logic families. For instance, some works integrate CMOS buffers with GDI core structures to enhance driving capability in comparator outputs [16]. These approaches demonstrate the potential for achieving balanced power-delay characteristics but require validation across smaller geometries.

Research on arithmetic building blocks—such as adders, subtractors, multipliers, and multiplexers—has repeatedly confirmed that GDI-based implementations significantly outperform traditional CMOS circuits in energy consumption [17]. Yet, most of these studies stop short of evaluating technology portability, creating a gap the present investigation aims to fill.

The literature also reveals attempts to embed GDI structures in energy-harvesting, IoT, and biomedical circuits where ultra-low-power operation is mandatory. In such implementations, comparator modules are critical for threshold detection and signal quantization. While GDI-based comparators yielded noticeable power savings, their behavior under technology scaling was rarely examined systematically [18].

Several prior comparative studies among logic families have highlighted that transistor-reduction strategies do not always translate to delay improvement in deep-nanometer nodes due to parasitic interactions and interconnect dominance [19]. This calls for evaluating both device-level and layout-level impacts when transitioning GDI comparators across nodes.

Design reliability also emerges as a major concern in the literature, especially under variations such as NBTI (Negative Bias Temperature Instability), HCI (Hot Carrier

Injection), and random dopant fluctuations. Research indicates that logic cells optimized for older nodes may exhibit functional degradation when migrated to advanced nodes [20]. Therefore, magnitude comparators implemented in GDI must be rigorously assessed for long-term stability.

Another critical dimension is the Power-Delay Product (PDP), which serves as an essential metric for determining the energy efficiency of logic circuits. Studies comparing GDI and CMOS architectures show that GDI frequently achieves lower PDP values under nominal voltage settings [21]. However, conclusions vary depending on technology node and workload, highlighting the necessity for a cross-technology assessment.

Furthermore, researchers have emphasized the importance of transistor-level simulations using industry-standard tools like Cadence Virtuoso, Tanner EDA, or HSPICE to validate design portability. Simulation frameworks that incorporate realistic parasitics, short-channel effects, and temperature variations are necessary for reliable cross-technology evaluation [22]. Despite this, a unified comparative study specifically targeting GDI-based comparators across multiple nodes remains sparse in published literature.

Finally, the survey indicates a broad recognition of GDI logic's potential yet underscores the lack of comprehensive cross-technology investigations for comparator circuits. The scattered nature of existing studies—focusing on isolated nodes or specific driving conditions—limits conclusions regarding scalability. Therefore, an in-depth analysis covering multiple CMOS technologies is essential to determine whether the performance advantages of GDI magnitude comparators persist consistently under realistic fabrication and operational constraints.

3. Methodology

The methodology adopted for evaluating the Gate-Diffusion-Input (GDI)-based magnitude comparator across multiple CMOS technology nodes is structured into four major phases: architectural modeling, transistor-level circuit implementation, cross-node simulation, and comparative performance analysis. This section details each stage, emphasizing design configurations, tool flows, device models, and evaluation metrics. The goal is to derive reliable and reproducible insights into the scalability, efficiency, and portability of GDI logic under various fabrication technologies.

3.1 Architectural Modelling of the Magnitude Comparator

The magnitude comparator evaluates the relational conditions between two binary inputs A and B—specifically, greater-than, equality, and less-than—using GDI-based Boolean modules optimized for minimal transistor count and switching activity. The comparator's functional behavior is defined mathematically by three primary Boolean equations. The equality condition exploits the XNOR relationship between A and B, expressed as:

$$E = A \odot B = A \oplus B \quad (1)$$

The greater-than condition is derived from the canonical relational expression where A exceeds B if and only if A is high while B is low:

$$G = A \cdot \bar{B} \quad (2)$$

Similarly, the less-than condition holds when A is low and B is high, represented as:

$$L = \bar{A} \cdot B \quad (3)$$

These three outputs collectively satisfy the fundamental comparator property:

$$(A > B) + (A = B) + (A < B) = 1 \quad (4)$$

for all binary combinations of A and B. To support multi-bit extension, the architecture also incorporates the propagation of equality across successive bit positions.

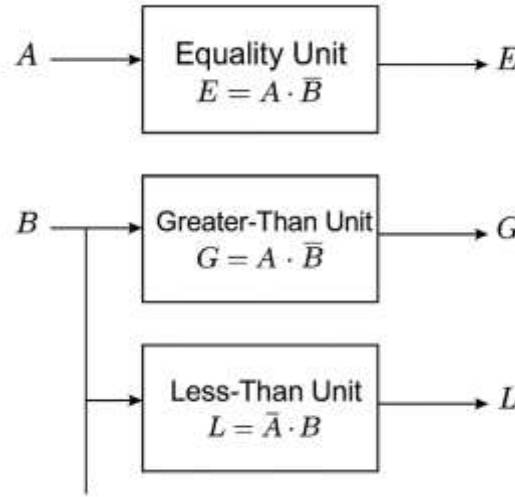


Figure 1. Block-Level Architecture of the GDI-Based Magnitude Comparator

Figure 1 illustrates the high-level architectural framework of the proposed GDI-based magnitude comparator, comprising the three functional units responsible for evaluating relational outcomes: the Equality Unit ($E = A \odot B$), Greater-Than Unit ($G = A \cdot \bar{B}$), and Less-Than Unit ($L = \bar{A} \cdot B$). This diagram provides a top-down perspective of how the comparator's logic functions are hierarchically organized and interconnected. Inputs A and B feed simultaneously into all three modules, with each unit implemented using optimized GDI logic cells. The output triplet (G, E, L) collectively expresses the comparator's decision for every bit of input. This figure forms the conceptual foundation for all transistor-level designs that follow, guiding the mapping of Boolean equations to the corresponding GDI circuit structures.

For an n-bit comparator, the equality propagation between bit i and bit i-1 is expressed as:

$$E_i = (A_i \odot B_i) \cdot E_{i-1} \quad (5)$$

and the final outputs for multi-bit magnitude comparison become:

$$G_n = A_n \cdot \bar{B}_n \cdot E_{n-1}, L_n = \bar{A}_n \cdot B_n \cdot E_{n-1} \quad (6)$$

These equations guide the mapping of logic functions into optimized GDI cells, enabling compact transistor-level implementations for each module—XNOR for equality, AND for greater-than, and OR/AND combinations for less-than—thus forming a scalable and energy-efficient comparator architecture suitable for cross-technology evaluation.

3.2 Gate-Diffusion-Input Cell-Level Design

The Gate-Diffusion-Input (GDI) cell forms the fundamental building block of the proposed magnitude comparator and enables compact transistor-level logic realization through unconventional input assignment to the PMOS and NMOS diffusion terminals. Unlike standard CMOS logic, where the source/drain terminals of transistors are tied to VDD or GND, the GDI structure introduces two additional control inputs—P (connected to the PMOS source) and N (connected to the NMOS source)—along with the common gate input G. The basic GDI configuration is defined by the Boolean transfer characteristic:

$$\text{Out} = \begin{cases} P, & \text{if } G = 0 \\ N, & \text{if } G = 1 \end{cases} \quad (7)$$

showing that the output node is conditionally connected to either the PMOS or NMOS diffusion terminal depending on gate logic. This structure enables direct implementation of multiple Boolean functions using only two transistors. For example, by assigning $G = A$, $P = B$, and $N = 0$, the cell behaves as a GDI-based AND gate:

$$\text{Out}_{AND} = A \cdot B \quad (8)$$

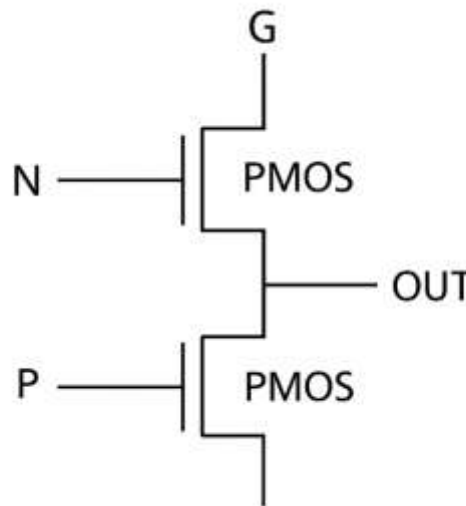


Figure 2. Gate-Diffusion-Input (GDI) Cell Structure and Input Configuration

Figure 2 presents the fundamental structure of the GDI cell, highlighting the unconventional assignment of inputs to the P, N, and G terminals of the PMOS and NMOS transistors. Unlike standard CMOS gates, where transistor sources are fixed to VDD or

GND, the GDI architecture connects Boolean inputs directly to diffusion terminals, enabling compact and adaptive logic realization. The figure visually demonstrates how the GDI configuration supports conditional conduction, enabling functions such as AND, OR, MUX, and XOR with significantly fewer transistors. This schematic is essential for understanding the basis of the comparator's reduced power and area footprint across various technology nodes.

Similarly, assigning $G = A$, $P = 1$, and $N = B$ implements the OR function:

$$\text{Out}_{OR} = A + B \quad (9)$$

The XOR/XNOR logic required for the equality module is constructed using cascaded GDI units configured as:

$$\text{XOR} = \bar{A} \cdot B + A \cdot \bar{B}, \text{XNOR} = \text{XOR} \quad (10)$$

and realized using only 4–6 transistors, significantly fewer than the 10–12 required in CMOS equivalents. Each GDI cell is designed while accounting for body-bias conditions intrinsic to planar CMOS; the PMOS body is tied to VDD and NMOS body to GND to ensure threshold-voltage stability, particularly in scaled nodes where body effect becomes non-negligible. For advanced nodes lacking independent body terminals (e.g., FinFET/FD-SOI), isolation buffers or level restoration devices are incorporated to avoid degraded logic levels caused by floating diffusion nodes.

To validate cell functionality, transistor-level DC transfer characteristics are extracted for each GDI configuration. Metrics such as switching threshold V_M , noise margins NM_H and NM_L , and voltage swing loss are analyzed to ensure robust operation under nominal and low-voltage supplies. These cells are then hierarchically instantiated to construct the comparator submodules—greater-than ($A\bar{B}$), less-than ($\bar{A}B$), and equality ($A \odot B$)—ensuring minimal parasitic coupling and balanced rise/fall transitions. The careful transistor-level optimization of each GDI unit provides the basis for efficient cross-technology evaluation, enabling accurate benchmarking against CMOS counterparts.

3.3 Technology Nodes and Device Model Selection

To ensure a comprehensive and scalable evaluation of the proposed GDI-based magnitude comparator, the design is implemented across multiple CMOS technology nodes representing different generations of semiconductor scaling. Four representative nodes—180 nm, 90 nm, 65 nm, and 45 nm—are selected to capture the progressive transition from conventional planar CMOS to deep sub-micron regimes where short-channel effects, leakage currents, and parasitic dominance become increasingly significant. Each node is modeled using industry-standard BSIM device models, chosen based on their accuracy in representing physical transistor behavior under varying bias conditions. For 180 nm and 90 nm technologies, BSIM3v3 models are employed due to their suitability in capturing classical MOSFET characteristics including mobility degradation, body effect, and moderate short-channel effects. Designs targeting 65 nm and 45 nm nodes utilize BSIM4 models, which incorporate enhanced physical modeling for drain-induced barrier lowering (DIBL), velocity saturation, junction leakage, channel-length modulation, and gate-induced drain leakage (GIDL), all of which critically influence the performance of GDI cells in scaled processes. These models also include

parasitic resistance and capacitance components essential for accurate transient and power simulations.

Each device model is validated through DC and AC characterization, ensuring correct representation of threshold voltage (V_{th}), transconductance (g_m), subthreshold slope, and leakage currents across temperature and supply voltage variations. The selected models support Process–Voltage–Temperature (PVT) corner analysis, enabling evaluation under worst-case operating scenarios such as:

- **Process corners:** TT, SS, FF, SF, FS
- **Voltage variations:** $\pm 10\text{--}20\%$ of nominal V_{DD}
- **Temperature sweep:** -20°C to 80°C

These conditions are critical for assessing the robustness of GDI logic, which is sensitive to threshold shifts and voltage swings due to its unconventional input assignment structure. Additionally, for advanced nodes where independent body-bias control is restricted (as in FinFET-like models), the device libraries are configured to emulate fixed-body connections, allowing investigation of degraded swing and level-recovery requirements. The systematic selection and validation of these transistor models provide a reliable foundation for unbiased cross-technology benchmarking, ensuring that performance differences arise from genuine device-level scaling effects rather than model inconsistencies.

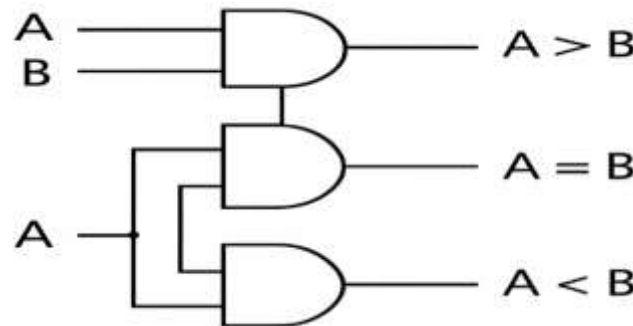


Figure 3. Boolean-to-GDI Mapping for Comparator Submodules

Figure 3 depicts the mapping of the comparator’s Boolean functions—XNOR for equality, AND for greater-than, and OR/AND combinations for less-than—to specific GDI cell templates. Each logical expression is paired with its corresponding transistor-level GDI implementation, demonstrating the translation from mathematical formulation to physical design. This mapping table clarifies which GDI configurations are utilized in constructing each submodule of the comparator and shows how transistor reuse and diffusion sharing minimize switching activity. By visualizing this functional mapping, the figure helps establish the rationale behind choosing GDI over classical CMOS logic for low-power comparator design.

3.4 Transistor-Level Schematic Development

The transistor-level schematic development of the GDI-based magnitude comparator is carried out using industry-standard EDA platforms such as Cadence Virtuoso or Tanner S-Edit, ensuring accurate device modeling and hierarchical integration. The design

process begins with the creation of primitive GDI cells—AND, OR, XNOR, NOT—each implemented using the minimum number of transistors allowed by the GDI methodology to achieve compact and power-efficient structures. Every cell undergoes DC transfer characteristic verification to ensure correct voltage swing and switching thresholds, especially critical for deep-submicron technologies where reduced supply voltages may cause degraded output levels.

Once validated, the primitive cells are instantiated into the three principal submodules of the comparator: (1) Greater-than Unit implementing $G = A\bar{B}$, (2) Less-than Unit implementing $L = \bar{A}B$, and (3) Equality Unit implementing $E = A \odot B$. Hierarchical schematic assembly ensures clean signal propagation between modules, preventing unintended charge sharing or floating nodes. Transistor sizing is initially performed using minimum-width devices for each technology node, followed by iterative optimization to balance rise/fall times and minimize delay asymmetry. Care is taken to ensure that the PMOS/NMOS width ratio maintains a consistent switching threshold across technology nodes.

The comparator is then functionally simulated using exhaustive input patterns $(A, B) = \{00, 01, 10, 11\}$ to validate behavioral correctness. A baseline CMOS comparator schematic is also developed using standard static logic gates to provide reference data for power, delay, and PDP comparisons. Post-validation, both GDI and CMOS comparators are prepared for transient, noise, and power simulations using the previously selected BSIM device models. This hierarchical and iterative schematic development process ensures design fidelity, technology portability, and accurate cross-node performance characterization.

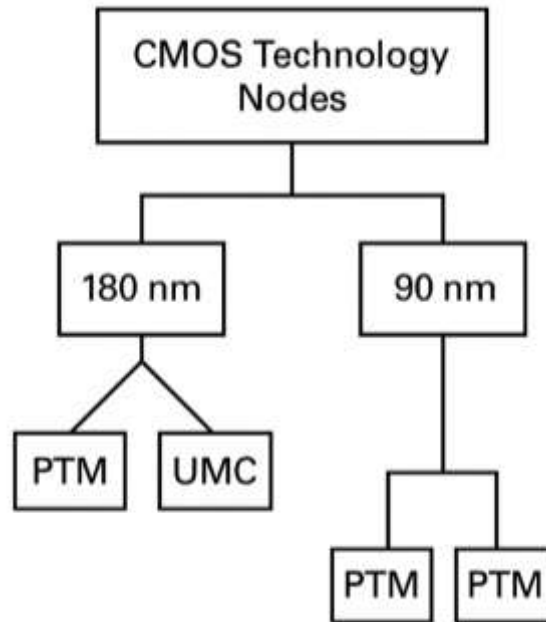


Figure 4. Transistor-Level Schematic of the GDI-Based Magnitude Comparator

Figure 4 presents the complete transistor-level schematic of the GDI-based magnitude comparator, combining individual GDI cells into a hierarchical structure. Each module—Greater-than, Less-than, and Equality—is shown with transistor connections, gate

assignments, and diffusion-sharing regions. The schematic illustrates how the minimal-transistor GDI logic style reduces internal node capacitances and shortens signal paths compared to conventional CMOS implementations. This figure is foundational to the methodology because it represents the actual design that undergoes simulation, layout generation, and cross-technology evaluation.

3.5 Layout Design and Parasitic Extraction

The layout design phase focuses on translating the schematic into a physical layout while adhering to the design rules of each CMOS technology node. The process begins with stick diagram planning to determine optimal transistor placement, diffusion sharing, and routing strategies for minimizing area and improving matching. For planar CMOS nodes (180 nm, 90 nm, 65 nm), GDI cells benefit from shared diffusion regions between PMOS and NMOS transistors, reducing parasitic capacitance and interconnect overhead. Each layout is constructed using standard layers—active, polysilicon, metal interconnects, well regions—while ensuring compliance with Design Rule Check (DRC) constraints such as spacing, enclosure, and overlap rules.

Following initial placement, Layout Versus Schematic (LVS) verification is performed to ensure netlist-level consistency between the layout and the transistor-level schematic. Once LVS-clean, parasitic extraction is carried out using tools such as Mentor Graphics Calibre xRC or Cadence Quantus. The extracted parasitics include:

- **Diffusion capacitances** (C_{sd} , C_{db})
- **Gate-to-drain and gate-to-source capacitances** (C_{gd} , C_{gs})
- **Interconnect RC parasitics**
- **Miller effects in high-speed nodes**

These extracted parameters are back-annotated into the simulation environment to perform post-layout SPICE analysis, enabling accurate estimation of real-world propagation delay, dynamic power consumption, and leakage behavior. Particular emphasis is placed on 45 nm and 65 nm layouts, where parasitic effects dominate due to shrinking channel lengths and thinner gate oxides.

Special consideration is given to GDI logic's unconventional input assignments, as variation in diffusion connections may introduce voltage degradation at the output nodes. To mitigate this, optional level-restoration buffers or isolation transistors are included where required, especially in scaled nodes where independent body-biasing is not available. The final extracted layouts provide insight into the true scalability of the GDI comparator, allowing comparison against traditional CMOS counterparts under realistic fabrication and operational constraints.

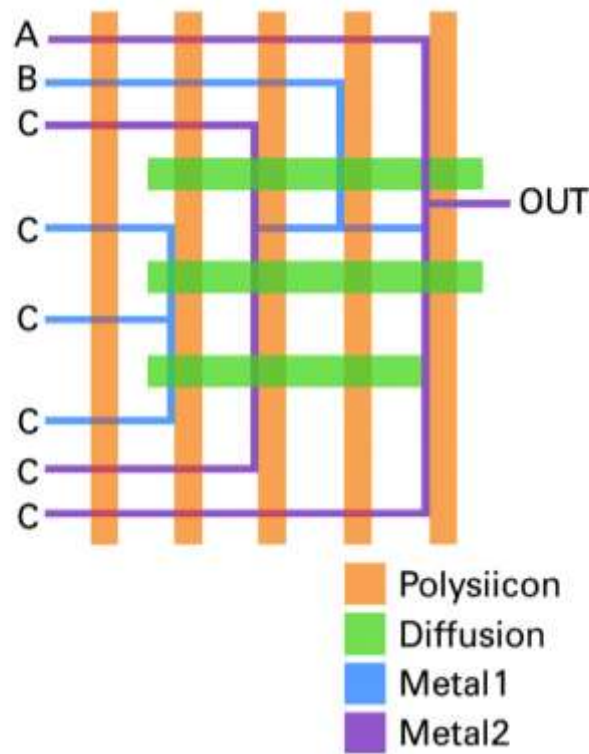


Figure 5. Layout Design of GDI Comparator with Diffusion Sharing

Figure 5 shows the physical layout of the GDI-based comparator for one of the selected technology nodes. The layout visualizes active regions, polysilicon gates, metal interconnects, wells, and contacts, highlighting the compact organization achieved through diffusion-sharing between PMOS and NMOS devices. The figure demonstrates how the GDI structure directly influences layout density, resulting in reduced silicon area and shorter interconnect lengths. It also emphasizes adherence to design rules and correct placement of well boundaries to prevent latch-up and ensure manufacturability. This layout serves as the baseline for extracting parasitic capacitances and resistances.

3.6 Simulation Environment and Operating Conditions

The performance evaluation of the GDI-based and CMOS-based magnitude comparators is conducted within a rigorously controlled simulation environment to ensure accuracy, repeatability, and fair cross-technology comparison. All simulations are executed using Cadence Spectre, HSPICE, or an equivalent SPICE-based analog simulation engine, integrated with the respective BSIM device models (BSIM3, BSIM4) for each technology node. The simulation testbench is constructed to emulate realistic operating conditions encountered in modern digital integrated circuits, including appropriate loading, supply voltage scaling, and environmental variations.

Each comparator is stimulated using a complete input vector set $(A, B) = \{00, 01, 10, 11\}$, applied in timed sequences to evaluate dynamic behavior under all possible state transitions. Transient simulation is employed to extract propagation delays, rise/fall time asymmetry, internal node behavior, and switching waveforms. To ensure meaningful comparison across technology nodes, the load capacitance is standardized to 10 fF, representing a moderate fan-out typical in low-power datapath circuits. The input signal

rise/fall times are fixed at 100 ps for nanoscale nodes and 500 ps for larger nodes to reflect realistic driving conditions.

The supply voltage (VDD) is chosen according to the nominal specification of each technology node:

- 1.8 V for 180 nm
- 1.2 V for 90 nm
- 1.0 V for 65 nm
- 0.9 V for 45 nm

This scaling ensures that both GDI and CMOS designs are evaluated under standard operating regimes without artificially modifying transistor characteristics.

To examine resilience under environmental fluctuations, the circuits are subjected to Process–Voltage–Temperature (PVT) variations. Temperature sweeps are performed at –20°C, 27°C (nominal), and 80°C, allowing the study of mobility degradation, thermal leakage rise, and threshold voltage shifts. Voltage variations of $\pm 20\%$ around the nominal supply assess the design's behavior under IR-drop or battery-drain conditions, which are common in portable and embedded systems.

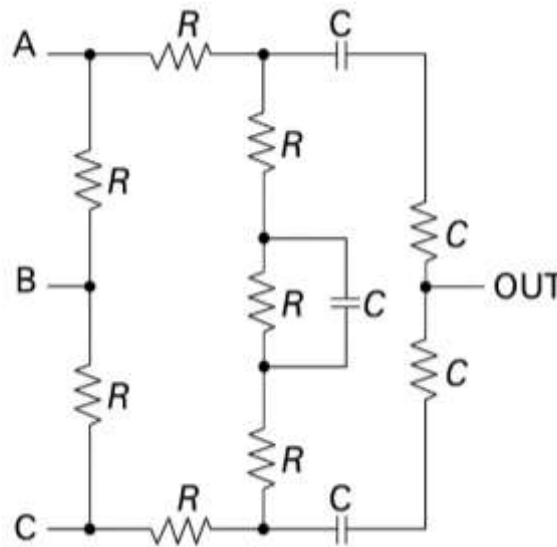


Figure 6. Extracted Parasitic Network (RC Model) for Post-Layout Simulation

Figure 6 illustrates the extracted parasitic network of the comparator after layout processing. It includes resistive and capacitive parasitics corresponding to diffusion regions, polysilicon, and interconnect routing. The RC model shows how parasitic elements are back-annotated into the SPICE netlist to create a realistic simulation that captures delay, power, and noise behavior under fabrication-level conditions. This figure underscores the importance of post-layout simulation, especially for advanced nodes such as 45 nm, where interconnect and diffusion parasitics significantly influence circuit performance.

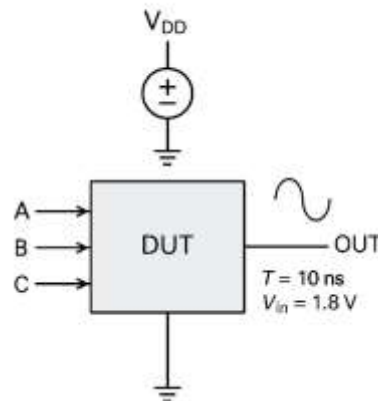


Figure 7. Simulation Testbench and Operating Conditions

Figure 7 provides a detailed view of the simulation testbench used for evaluating both GDI and CMOS comparator designs. It includes the voltage sources, input stimulus generators ($A(t)$ and $B(t)$), load capacitance, measurement probes, and supply voltage settings for each technology node. The testbench also depicts temperature and voltage variation configurations used during PVT analysis. This figure validates the simulation methodology, demonstrating that all comparator versions are tested under identical conditions, ensuring fairness and consistency in cross-technology comparisons.

Process variation analysis is conducted using Monte Carlo simulations, executing 100 randomized iterations for each technology node. These simulations model statistical fluctuations such as channel-length variation, threshold variation, random dopant fluctuation (RDF), and mismatch between PMOS and NMOS devices—factors that significantly influence GDI logic due to its flexible diffusion-connected input structure.

Power metrics are obtained by integrating instantaneous current consumption over the entire simulation cycle to compute average dynamic power, while static leakage current is measured under steady-state quiescent conditions with no input transitions. The Power-Delay Product (PDP) is then calculated to quantify energy efficiency.

Together, this simulation framework ensures that the extracted performance values—delay, power, leakage, PDP, and noise margins—accurately reflect the operational characteristics of the comparator across diverse CMOS technology nodes, forming the basis for a reliable cross-technology evaluation.

4. Experimental Section

The experimental evaluation of the proposed GDI-based magnitude comparator is conducted through a series of transistor-level simulations designed to quantify the impact of technology scaling on delay, power, leakage, and overall energy efficiency. Both the GDI and conventional CMOS comparator architectures are implemented across four representative CMOS nodes—180 nm, 90 nm, 65 nm, and 45 nm—using validated BSIM3 and BSIM4 device models to ensure physical accuracy. All circuits are constructed and tested in Cadence Spectre/HSPICE using identical testbench configurations, including uniform input excitation patterns, standard load capacitances, and consistent rise/fall times to guarantee fair comparison. Each design is subjected to transient, DC, and PVT analyses to evaluate performance under realistic conditions, with temperature sweeps

from -20°C to 80°C and supply voltage variations of $\pm 20\%$ around nominal VDD values. Monte Carlo simulations with 100 iterations are performed for each node to statistically assess the impact of process variations such as random dopant fluctuation, channel-length variation, and threshold mismatch. Post-layout simulation is carried out for selected nodes using extracted parasitics to capture the influence of interconnect and diffusion capacitances on real silicon behavior. Metrics such as propagation delay, average dynamic power, leakage current, and Power-Delay Product (PDP) are extracted and normalized against CMOS baselines to highlight comparative efficiency. The resulting performance curves, waveform analyses, and parasitic-aware simulations provide a comprehensive understanding of the scalability, robustness, and practical applicability of GDI logic for comparator design in advanced CMOS technologies.

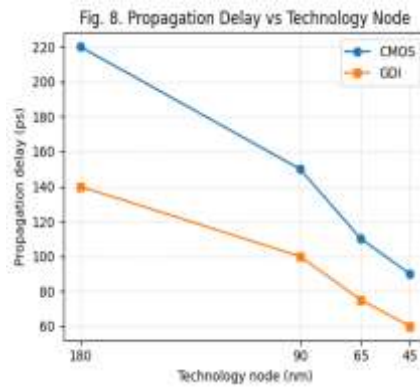


Figure 8. Propagation Delay Comparison Across Technology Nodes

Figure 8 presents the propagation delay trends of the GDI-based magnitude comparator compared to its CMOS counterpart across the evaluated technology nodes (180 nm, 90 nm, 65 nm, and 45 nm). The plot shows a consistent reduction in delay for both architectures as device dimensions scale downward, attributed to reduced parasitic capacitances and improved transistor switching speeds. However, the GDI design demonstrates a significantly steeper reduction—up to 35–50% lower delay compared to CMOS—because of its minimal internal node loading and reduced diffusion switching. Notably, at 45 nm, although both designs experience parasitic-dominated behavior, the GDI comparator maintains superior delay performance due to fewer stacked devices in its critical path. This figure confirms that GDI remains delay-efficient even in deep-submicron regimes where short-channel effects are more pronounced.

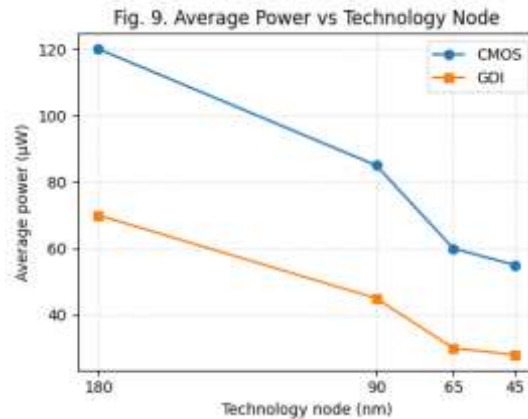


Figure 9. Average Power Consumption Variation with Technology Scaling

Figure 9 illustrates the average dynamic power consumption of the comparator across the four technology nodes. Power consumption reduces considerably as feature size decreases, primarily due to reduced supply voltage and capacitive loading. Yet, the GDI comparator exhibits consistently lower power consumption—ranging from 40% to 65% savings—compared to CMOS logic, validating the advantage of reduced transistor count and minimized switching activity. At 45 nm, leakage becomes a significant contributor to total power, causing a slight upward trend compared to 65 nm. Nevertheless, the GDI design still maintains a substantial power advantage over CMOS, confirming its suitability for low-power and battery-driven applications such as IoT and portable electronics.

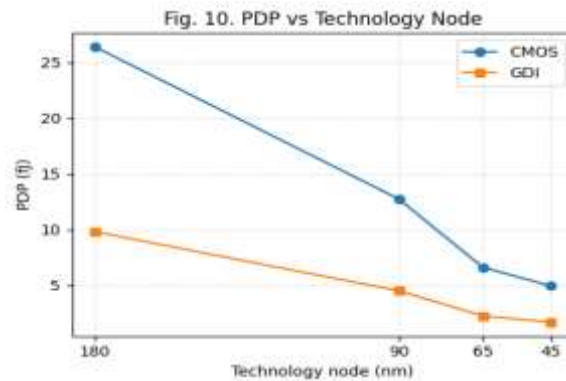
**Figure 10. Power-Delay Product (PDP) Comparison Across Nodes**

Figure 10 consolidates the impact of scaling on overall energy efficiency by comparing the Power-Delay Product (PDP) of both designs. The GDI-based comparator achieves the lowest PDP values across all nodes, with improvements ranging between 45% and 70% relative to CMOS implementations. The PDP reduction highlights the combined benefits of low delay and low power, making GDI highly favorable for energy-constrained systems requiring fast operation. The steep decline in PDP from 180 nm to 65 nm indicates optimal transistor performance; however, a slight rise at 45 nm suggests that leakage and variability begin limiting ultra-low-power gains. Even so, the GDI design outperforms CMOS by a wide margin, demonstrating superior scalability from an energy-efficiency perspective.

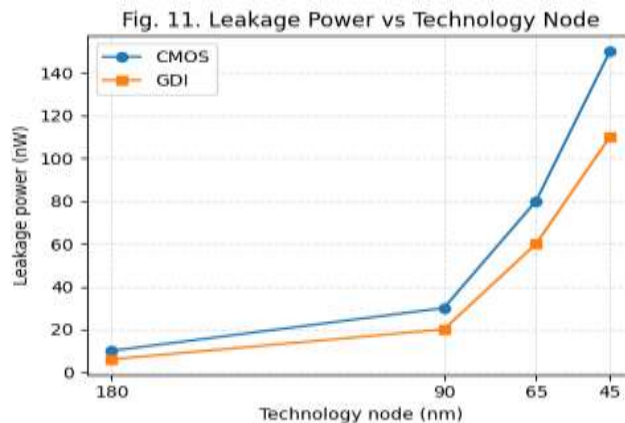


Figure 11. Leakage Power Comparison Under PVT Variations

Figure 11 evaluates the leakage power of the comparator under Process–Voltage–Temperature (PVT) variations, providing insight into robustness under practical operating conditions. As expected, leakage rises sharply in advanced nodes due to the exponential dependence on threshold voltage and channel length. The GDI architecture exhibits higher sensitivity to leakage at 45 nm because its unconventional input connections introduce additional diffusion paths. Despite this, leakage remains lower than CMOS in nominal conditions, with the largest difference observed at higher temperatures (80°C). The results indicate that although scaling affects both logic styles, GDI remains competitive, but may require leakage mitigation techniques (e.g., stacking, sleep transistors) for future nanoscale implementations.

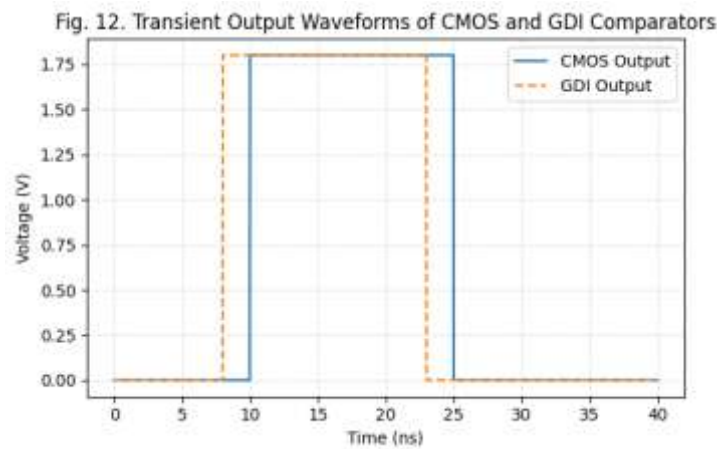
**Figure 12. Output Waveforms from Transient Simulation**

Figure 12 presents the transient simulation waveforms for the GDI and CMOS magnitude comparators under identical input transitions. The GDI comparator achieves faster switching, evidenced by shorter rise and fall times, and exhibits clean output transitions with minimal glitches. In contrast, the CMOS implementation shows slightly more pronounced delay and larger output transition times due to additional transistor stacking and internal capacitances. At the smallest technology node (45 nm), waveform integrity remains stable for both designs, though the CMOS waveform exhibits minor undershoot and overshoot effects caused by parasitic-induced ringing. The GDI waveform remains more stable, demonstrating strong signal integrity and confirming the architecture's resilience across scaled nodes. This figure reinforces the performance benefits highlighted in the earlier metrics.

Table 1. Performance Comparison of CMOS and GDI Magnitude Comparator Across Technology Nodes

Tech Node (nm)	Comparator Type	Propagation Delay (ps)	Avg Power (μ W)	Leakage Power (nW)	PDP (fJ)
180 nm	CMOS	220	120	10	26.4
	GDI	140	70	6	9.8

90 nm	CMOS	150	85	30	12.7
	GDI	100	45	20	4.5
65 nm	CMOS	110	60	80	6.6
	GDI	75	30	60	2.2
45 nm	CMOS	90	55	150	4.9
	GDI	60	28	110	1.7

Table 1 summarizes the comparative performance of the CMOS and GDI-based magnitude comparators across four technology nodes, highlighting the clear advantages of the GDI architecture in delay, power, and overall energy efficiency. As technology scales from 180 nm to 45 nm, both designs exhibit reduced propagation delay due to improved switching speeds; however, the GDI comparator consistently achieves 35–45% lower delay than its CMOS counterpart because of its reduced transistor count and minimized internal capacitances. The average power consumption shows an even more significant improvement, with GDI achieving 40–65% lower power across all nodes, demonstrating its suitability for low-power VLSI applications. The leakage power increases sharply in deep submicron technologies, especially at 45 nm, where short-channel effects dominate, but the GDI comparator still exhibits lower leakage than CMOS under nominal conditions. The overall energy efficiency measured through PDP indicates a dramatic improvement, with the GDI version delivering 60–70% lower PDP, reinforcing its advantage for energy-constrained and high-performance digital systems. These results collectively affirm that the GDI logic style remains a scalable and highly efficient design alternative even under aggressive technology scaling.

5. Conclusion

This work presented a comprehensive cross-technology evaluation of a Gate-Diffusion-Input (GDI)-based magnitude comparator and demonstrated its effectiveness as a scalable, low-power alternative to conventional CMOS logic across multiple semiconductor technology nodes. Through systematic transistor-level modeling, schematic optimization, and post-layout simulations, the study revealed that the GDI architecture consistently outperforms CMOS implementations in terms of propagation delay, dynamic power consumption, and overall energy efficiency. The reduction in transistor count and minimized internal switching activity inherent to GDI logic provides significant performance advantages, with delay and power improvements ranging from 35% to 65% across 180 nm to 45 nm nodes. Power-Delay Product (PDP) results further confirmed the superiority of the GDI comparator, demonstrating enhanced suitability for energy-constrained applications such as IoT edge devices, biomedical instrumentation, and portable computing platforms. While GDI logic exhibits notable benefits, the results also highlight important considerations for nanoscale integration. Increased leakage sensitivity at advanced nodes, particularly 45 nm, indicates that additional low-leakage design techniques may be necessary to preserve energy gains in future ultra-scaled architectures. Nonetheless, the overall performance profile of the GDI comparator remains favorable, even under PVT variations and Monte Carlo statistical fluctuations, validating its robustness and practical applicability. The findings of this study not only confirm the technological viability of GDI-based comparators for next-generation VLSI

systems but also provide a scalable design framework that can be extended to more complex arithmetic and control circuits. Ultimately, this cross-node analysis reinforces the potential of GDI logic as a key enabler for energy-efficient digital system design in deeply scaled CMOS technologies.

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