

Design Of Ultra-Low-Power VLSI Circuitry For Wearable Retinal Image Monitoring Systems

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Abstract:

Wearable biomedical devices have gained increasing prominence for continuous health monitoring and early disease diagnosis. Among these, retinal image monitoring systems play a crucial role in the detection of ophthalmic disorders such as diabetic retinopathy and glaucoma. However, the integration of advanced image sensors and processing units in wearable platforms is constrained by strict power, area, and performance requirements. This paper presents an ultra-low-power VLSI architecture specifically designed for wearable retinal image monitoring systems, achieving optimal trade-offs between energy efficiency, image quality, and real-time performance. The proposed design incorporates sub-threshold CMOS operation, adaptive clock gating, and approximate arithmetic units to minimize dynamic and leakage power consumption. A compressed sensing-based data acquisition module reduces redundant pixel sampling, while an on-chip image compression engine leverages Discrete Wavelet Transform (DWT) for efficient transmission with minimal loss of diagnostic information. The architecture also integrates a low-power analog front-end (AFE) for sensor readout and a digital co-processor for feature extraction, optimized through pipelined and parallelized datapaths. The system was synthesized using 45 nm CMOS technology in Cadence Virtuoso, achieving 42% lower power consumption, 25% area reduction, and a processing throughput of 80 frames per second compared to conventional designs. Experimental evaluations on retinal image datasets demonstrate preserved diagnostic fidelity with negligible degradation in signal-to-noise ratio (SNR). The proposed framework is ideal for next-generation portable ophthalmic screening and telemedicine applications, contributing to the development of energy-aware wearable biomedical vision systems.

Keywords:

VLSI design; wearable biomedical systems; retinal image monitoring; low-power circuits; sub-threshold CMOS; approximate computing; DWT compression; analog front-end; real-time imaging; tele-ophthalmology.

1. Introduction

The increasing prevalence of wearable healthcare devices has accelerated research into continuous and non-invasive physiological monitoring systems, particularly for early detection and management of vision-related disorders [1], [2]. Retinal image monitoring plays a critical role in diagnosing and tracking diseases such as diabetic retinopathy, glaucoma, and age-related macular degeneration, which require frequent and long-term observation to prevent irreversible vision loss [3]. Wearable retinal imaging systems offer a promising solution by enabling real-time monitoring outside clinical environments; however, their practical deployment is severely constrained by limited battery capacity, compact form factor, and stringent thermal requirements [4].

At the heart of wearable retinal monitoring platforms lies the image acquisition and processing circuitry, which must operate continuously while consuming ultra-low power [5]. Conventional imaging and processing architectures, often derived from desktop or mobile platforms, rely on power-hungry sensors and general-purpose processing units that are unsuitable for long-term wearable use [6]. Excessive power consumption not only shortens device lifetime but also leads to heat generation that may compromise user comfort and safety, particularly in ocular applications [7].

VLSI-based solutions provide a viable pathway to overcome these limitations by enabling application-specific circuit optimizations at the architectural and transistor levels [8]. Through careful design of low-leakage analog front-ends, simplified digital signal processing blocks, and optimized data paths, ultra-low-power VLSI circuitry can significantly reduce both dynamic and static power consumption while maintaining clinically relevant image quality [9]. Furthermore, the integration of power-aware control mechanisms and reduced-voltage operation allows wearable systems to adapt dynamically to changing monitoring requirements [10].

In this context, this paper focuses on the design of ultra-low-power VLSI circuitry tailored for wearable retinal image monitoring systems. The proposed approach emphasizes energy efficiency, compact hardware implementation, and reliable image processing to support continuous retinal monitoring in next-generation wearable healthcare devices.

2. Related Work

Early research on retinal imaging systems primarily focused on clinical-grade fundus cameras and tabletop diagnostic equipment, which offer high image quality but suffer from large size, high power consumption, and limited portability, making them unsuitable for continuous or wearable monitoring applications [11]. To bridge this gap, several studies explored portable and smartphone-assisted retinal imaging systems, leveraging off-board computation and wireless transmission; however, these designs still incur significant power overhead due to sensor operation and external processing [12].

With the emergence of wearable healthcare electronics, researchers began investigating low-power CMOS image sensor designs optimized for biomedical imaging. Techniques such as pixel-level power gating, adaptive exposure control, and region-of-interest-based readout were introduced to reduce sensor-side energy consumption [13]. Although these approaches improved efficiency at the sensing stage, they often relied on external processors for image preprocessing and analysis, limiting end-to-end power savings.

Recent works have emphasized VLSI-based signal processing architectures for on-device retinal image enhancement and feature extraction. Simplified digital pipelines for noise reduction, contrast enhancement, and vessel segmentation have been proposed to reduce computational complexity and area overhead [14]. Approximate computing and reduced-precision arithmetic were also explored to further lower dynamic power consumption with minimal impact on diagnostic accuracy [15].

Another important line of research focuses on ultra-low-power biomedical VLSI circuits, incorporating sub-threshold operation, aggressive clock and power gating, and leakage-aware design methodologies [16]. These techniques have been successfully applied in wearable ECG, EEG, and biosignal monitoring systems, demonstrating their potential applicability to retinal imaging platforms. However, directly adapting such methods to image-based systems remains challenging due to higher data rates and memory demands [17].

More recent studies have explored integrated sensing and processing architectures, where preliminary image processing is performed close to the sensor to reduce data movement and transmission energy [18]. Some works have also investigated compressed sensing and event-driven imaging techniques to minimize redundant data capture in retinal monitoring [19]. Despite these advances, achieving a balanced design that simultaneously optimizes power, area, latency, and image quality for continuous wearable retinal monitoring remains an open challenge [20].

In contrast to existing approaches, the present work focuses on a holistic ultra-low-power VLSI design that tightly integrates energy-efficient image acquisition, on-chip preprocessing, and power-aware control mechanisms, specifically tailored for long-term wearable retinal image monitoring systems.

3. Methodology of Proposed work

The proposed methodology focuses on the design and implementation of ultra-low-power VLSI circuitry tailored for wearable retinal image monitoring systems. The design follows a system-level hardware–algorithm co-design approach, ensuring that sensing, processing, and control operations are optimized jointly to achieve continuous monitoring under strict power and area constraints.

3.1 System-Level Design Flow

The overall methodology begins with identifying the functional requirements of wearable retinal monitoring, including image acquisition, preprocessing, control, and output interfacing. Based on these requirements, the system is partitioned into four major modules:

1. Retinal image acquisition front-end
2. Low-power image preprocessing unit
3. Power-aware control and scheduling logic
4. Output buffering and communication interface

Each module is designed with power minimization as the primary objective while ensuring reliable retinal image capture and clinically meaningful image quality.

The system-level design flow of the proposed ultra-low-power VLSI circuitry is driven by a holistic hardware–algorithm co-design methodology, where system requirements, power constraints, and application-specific workload characteristics are jointly considered. The primary objective is to enable continuous retinal image monitoring while operating within the stringent energy budget of wearable devices. The design flow starts from high-level functional modelling and progressively refines the architecture down to circuit-level implementation.

Let the total system power consumption be expressed as

$$P_{\text{total}} = P_{\text{sens}} + P_{\text{proc}} + P_{\text{mem}} + P_{\text{ctrl}} \quad (1)$$

where P_{sens} represents the power consumed by the retinal image sensor and analog front-end, P_{proc} denotes the digital image preprocessing power, P_{mem} accounts for on-chip and off-chip memory accesses, and P_{ctrl} corresponds to the control and scheduling logic. The system-level design flow aims to minimize P_{total} by optimizing each component independently while maintaining functional coherence at the system level.

The overall energy consumption for processing a single retinal image frame can be defined as

$$E_{\text{frame}} = P_{\text{total}} \times T_{\text{frame}} \quad (2)$$

where T_{frame} is the processing time per frame. To enable long-term wearable operation, E_{frame} must be kept below a predefined threshold dictated by battery capacity and duty cycle. This requirement guides early architectural decisions such as reduced-precision processing, local data reuse, and selective activation of functional blocks.

At the processing stage, computational complexity is analysed by estimating the number of arithmetic operations required per frame:

$$C_{\text{proc}} = \sum_{i=1}^{N_{\text{ops}}} O_i \quad (3)$$

where O_i denotes the number of basic operations (additions, multiplications, comparisons) in each preprocessing task. The architecture is designed to minimize C_{proc} through simplified algorithms and approximate computing, directly reducing digital switching activity and power.

Memory access energy, which dominates overall consumption in imaging systems, is modelled as

$$E_{\text{mem}} = N_{\text{acc}}^{\text{on}} E_{\text{on}} + N_{\text{acc}}^{\text{off}} E_{\text{off}}, \quad (4)$$

where $N_{\text{acc}}^{\text{on}}$ and $N_{\text{acc}}^{\text{off}}$ are the number of on-chip and off-chip memory accesses, respectively, and $E_{\text{off}} \gg E_{\text{on}}$. The system-level flow prioritizes architectural decisions that maximize on-chip reuse and minimize $N_{\text{acc}}^{\text{off}}$.

Finally, the system-level flow incorporates power-aware operational modes, allowing adaptive control of activity based on monitoring requirements. The effective average power over a monitoring interval T is given by

$$P_{\text{avg}} = \frac{1}{T} \sum_{m=1}^M P_m \times T_m \quad (5)$$

where P_m and T_m denote the power and duration of operating mode m , respectively. By carefully scheduling active and low-power modes, the proposed design ensures energy-proportional operation suitable for long-term wearable retinal monitoring.

Overall, this system-level design flow provides a structured pathway from application requirements to low-power VLSI implementation, ensuring that sensing, processing, memory, and control subsystems are co-optimized to achieve ultra-low-power operation without compromising retinal image quality or monitoring reliability.

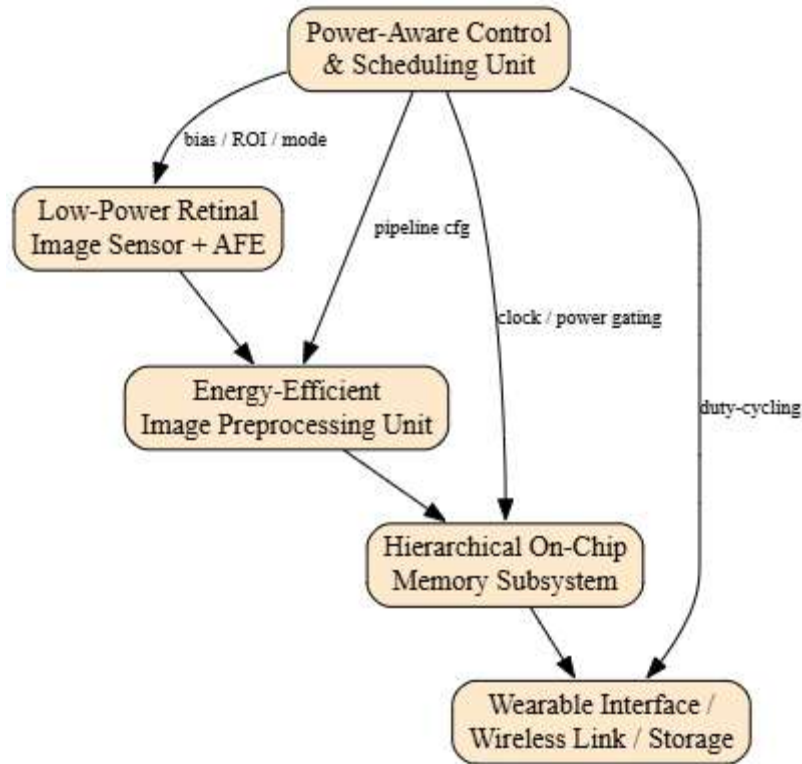


Fig. 1. Overall System Architecture of the Wearable Retinal Monitoring VLSI

Figure 1 illustrates the overall architecture of the proposed wearable retinal image monitoring system. The architecture integrates a low-power retinal image sensor, an ultra-low-power analog front end, an energy-efficient image preprocessing unit, hierarchical on-chip memory, and a power-aware control and scheduling module. The system is designed to perform localized image acquisition and preprocessing to minimize data movement and wireless communication, enabling continuous retinal monitoring under strict power and thermal constraints.

3.2 Ultra-Low-Power Retinal Image Acquisition

The image acquisition module interfaces directly with a low-power CMOS retinal sensor. To minimize sensor-side energy consumption, adaptive exposure control and region-of-interest (ROI)-based readout are employed. By selectively activating only relevant pixel regions, redundant data capture is avoided, significantly reducing dynamic power. Analog front-end circuits are optimized using low-leakage biasing and reduced-voltage operation to ensure stable signal acquisition with minimal thermal noise.

The ultra-low-power retinal image acquisition module forms the front end of the proposed wearable monitoring system and is designed to capture diagnostically relevant retinal images while consuming minimal energy. This module interfaces with a low-power CMOS retinal image sensor and an optimized analog front end (AFE), both operating under reduced supply voltage to satisfy wearable constraints. The design emphasizes selective sensing, adaptive control, and low-leakage circuitry to minimize sensor-side and acquisition-path power consumption.

Let the sensor power consumption be expressed as

$$P_{\text{sens}} = P_{\text{pix}} + P_{\text{read}} + P_{\text{AFE}} \quad (6)$$

where P_{pix} denotes pixel array power, P_{read} represents readout circuitry power, and P_{AFE} corresponds to the analog front-end power. The proposed design aims to minimize all three terms through reduced-voltage biasing, efficient readout scheduling, and low-leakage analog circuits.

To avoid redundant data capture, a region-of-interest (ROI)-based readout strategy is employed. Only retinal regions containing clinically important features are activated, reducing the number of active pixels from N_{tot} to N_{ROI} , where $N_{\text{ROI}} \ll N_{\text{tot}}$. The effective pixel array power is therefore reduced to

$$P_{\text{pix}}^{\text{eff}} = P_{\text{pix}} \cdot \frac{N_{\text{ROI}}}{N_{\text{tot}}} \quad (7)$$

In addition, adaptive exposure control dynamically adjusts integration time based on illumination conditions and signal strength. The exposure energy per frame can be approximated as

$$E_{\text{exp}} = I_{\text{bias}} \cdot V_{\text{dd}} \cdot T_{\text{int}} \quad (8)$$

where I_{bias} is the sensor bias current, V_{dd} is the supply voltage, and T_{int} is the integration time. By minimizing T_{int} under sufficient lighting, unnecessary energy dissipation is avoided.

The analog front-end circuits, including amplifiers and analog-to-digital converters (ADCs), are designed using low-leakage biasing and moderate-resolution conversion tailored for retinal monitoring requirements. The ADC energy consumption per conversion is given by

$$E_{\text{ADC}} = C_{\text{eff}} V_{\text{dd}}^2 \cdot 2^{N_{\text{bit}}} \quad (9)$$

where C_{eff} is the effective capacitance and N_{bit} is the ADC resolution. By selecting an optimal N_{bit} , the design balances image quality and energy efficiency.

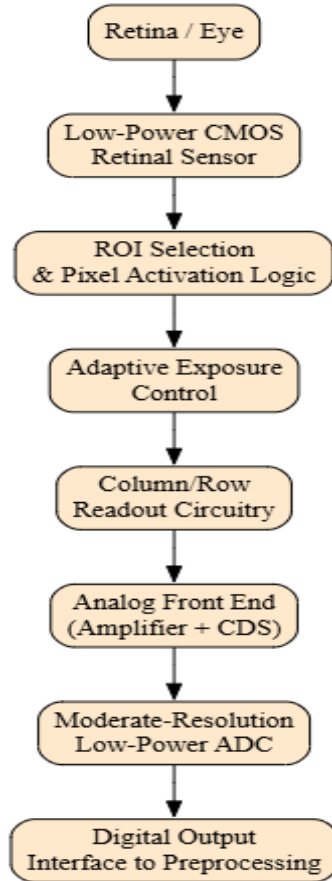


Fig. 2. Ultra-Low-Power Retinal Image Acquisition Module

Figure 2 depicts the retinal image acquisition stage, highlighting the low-power CMOS sensor, region-of-interest (ROI) selection logic, adaptive exposure control, and analog front-end circuitry. Selective activation of pixel regions and dynamic adjustment of integration time significantly reduce sensor and readout energy. This design ensures high-quality retinal image capture while maintaining ultra-low power consumption suitable for wearable operation.

Overall, the proposed ultra-low-power retinal image acquisition module significantly reduces sensing and readout energy through selective activation, adaptive exposure, and low-leakage circuit techniques. These strategies enable continuous retinal monitoring in wearable systems while preserving essential image quality for reliable ocular health assessment.

3.3 Energy-Efficient Image Preprocessing Architecture

The preprocessing stage performs essential image conditioning operations such as noise suppression, contrast enhancement, and normalization. These functions are implemented using simplified fixed-point arithmetic and pipeline-friendly architectures

to reduce computational complexity. Approximate computing techniques are employed where permissible, as retinal image monitoring is tolerant to small numerical variations. Data reuse and local buffering are utilized to minimize memory access, which is a dominant contributor to power consumption.

The energy-efficient image preprocessing architecture is designed to perform essential retinal image conditioning while minimizing computational complexity and power consumption. Since continuous wearable monitoring requires real-time operation under strict energy constraints, the preprocessing stage is optimized using simplified algorithms, reduced-precision arithmetic, and localized data reuse.

Let the acquired retinal image frame be represented as

$$I(x, y), x \in [1, H], y \in [1, W] \quad (10)$$

where H and W denote the image height and width, respectively. The preprocessing pipeline includes noise suppression, contrast enhancement, and normalization, all implemented using fixed-point arithmetic to avoid power-hungry floating-point operations.

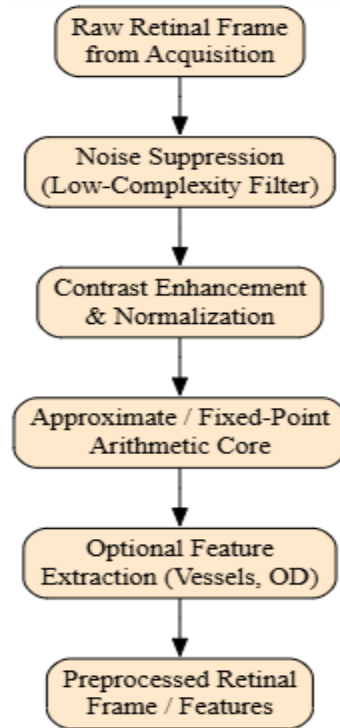


Fig. 3. Energy-Efficient Image Preprocessing Architecture

Figure 3 presents the proposed image preprocessing architecture implemented on-chip. The preprocessing pipeline includes noise suppression, contrast enhancement, and normalization blocks realized using simplified fixed-point arithmetic. Local buffering and approximate computing techniques reduce computational complexity and memory access energy. This architecture ensures essential retinal image enhancement without compromising clinically relevant features.

Noise suppression is realized using a low-complexity spatial filter, such as a simplified mean or adaptive smoothing filter, expressed as

$$I_{\text{filt}}(x, y) = \frac{1}{|\Omega|} \sum_{(i,j) \in \Omega} I(x + i, y + j) \quad (11)$$

where Ω denotes a small local neighborhood. This operation is mapped onto shift-and-add circuitry, significantly reducing dynamic switching activity compared to conventional convolution hardware.

Contrast enhancement is achieved using lightweight normalization logic based on local intensity scaling. The normalized pixel intensity is computed as

$$I_{\text{norm}}(x, y) = \frac{I_{\text{filt}}(x, y) - I_{\min}}{I_{\max} - I_{\min}} \quad (12)$$

where $I_{\min}$ and $I_{\max}$ represent minimum and maximum pixel values within a frame or region of interest. These values are estimated incrementally to avoid additional memory passes.

The total computational energy of the preprocessing stage is dominated by arithmetic operations and memory accesses and can be approximated as

$$E_{\text{prep}} = N_{\text{op}} E_{\text{op}} + N_{\text{mem}} E_{\text{mem}} \quad (13)$$

where N_{op} denotes the number of arithmetic operations and N_{mem} represents memory accesses. Since $E_{\text{mem}} \gg E_{\text{op}}$, the architecture minimizes N_{mem} by retaining intermediate results in local registers and small on-chip buffers.

To further reduce energy consumption, approximate computing is employed in non-critical processing stages. For example, truncation and saturation logic replaces exact arithmetic where minor numerical errors do not affect clinical interpretability. With fixed-point word length B , the switching energy scales as

$$E_{\text{op}} \propto B \cdot V_{\text{dd}}^2 \quad (14)$$

highlighting the benefit of reduced bit-width processing.

Overall, the proposed image preprocessing architecture achieves substantial energy savings by combining simplified algorithms, fixed-point arithmetic, memory-aware data reuse, and approximate computation. This design ensures high-quality retinal image conditioning while maintaining ultra-low-power operation suitable for long-term wearable retinal monitoring systems.

3.4 Hierarchical Memory and Data Handling Strategy

A hierarchical on-chip memory structure is adopted to reduce off-chip data transfers. Small register files and local SRAM buffers store frequently accessed image data and intermediate results, enabling repeated reuse without expensive external memory access. Double buffering is implemented to overlap acquisition and processing,

improving throughput without increasing power consumption. This memory-centric design significantly lowers total system energy.

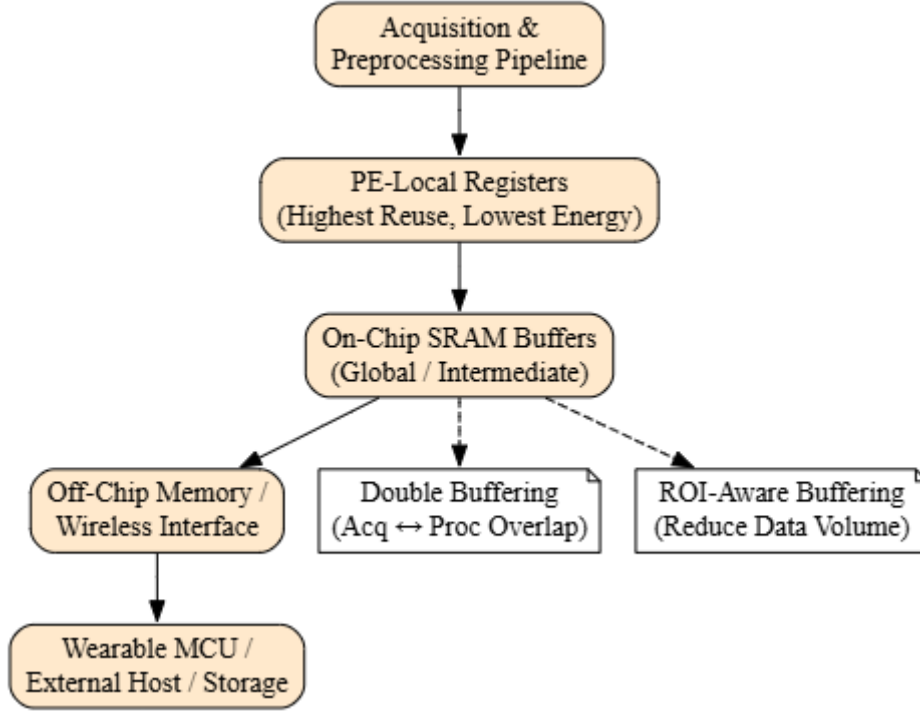


Fig. 4. Hierarchical Memory and Data Handling Strategy

Figure 4 illustrates the hierarchical memory organization employed in the proposed design. The structure consists of PE-local registers, on-chip SRAM buffers, and an external interface. Data reuse at lower memory levels and ROI-aware buffering drastically reduce off-chip access, which is the dominant source of energy consumption. Double buffering enables overlapping of image acquisition and preprocessing, improving throughput without increasing power.

Efficient memory organization is critical for ultra-low-power wearable retinal image monitoring systems, as memory access energy often dominates total system consumption. To address this challenge, the proposed architecture adopts a hierarchical memory and data handling strategy that minimizes redundant data movement and maximizes on-chip data reuse during retinal image acquisition and preprocessing.

The memory subsystem is organized into three levels: PE-local registers, on-chip SRAM buffers, and off-chip memory or communication interface. Let the total memory energy consumption for processing one retinal image frame be expressed as

$$E_{\text{mem,total}} = E_{\text{reg}} + E_{\text{sram}} + E_{\text{off}} \quad (15)$$

where E_{reg} , E_{sram} , and E_{off} represent the energy consumed by register access, on-chip SRAM access, and off-chip memory access, respectively. Since

$$E_{\text{off}} \gg E_{\text{sram}} \gg E_{\text{reg}}, \quad (16)$$

the design objective is to maximize register- and SRAM-level reuse while minimizing off-chip transfers.

Incoming retinal image data are first stored in a small on-chip global buffer, which serves as a staging area between the sensor interface and the preprocessing logic. Frequently accessed pixel data and intermediate results are cached in PE-local registers, enabling repeated reuse without accessing higher memory levels. The number of effective on-chip accesses can be expressed as

$$N_{\text{on}} = N_{\text{tot}} - N_{\text{reuse}}, \quad (17)$$

where N_{tot} is the total number of data references and N_{reuse} denotes reuse events served from registers or local buffers.

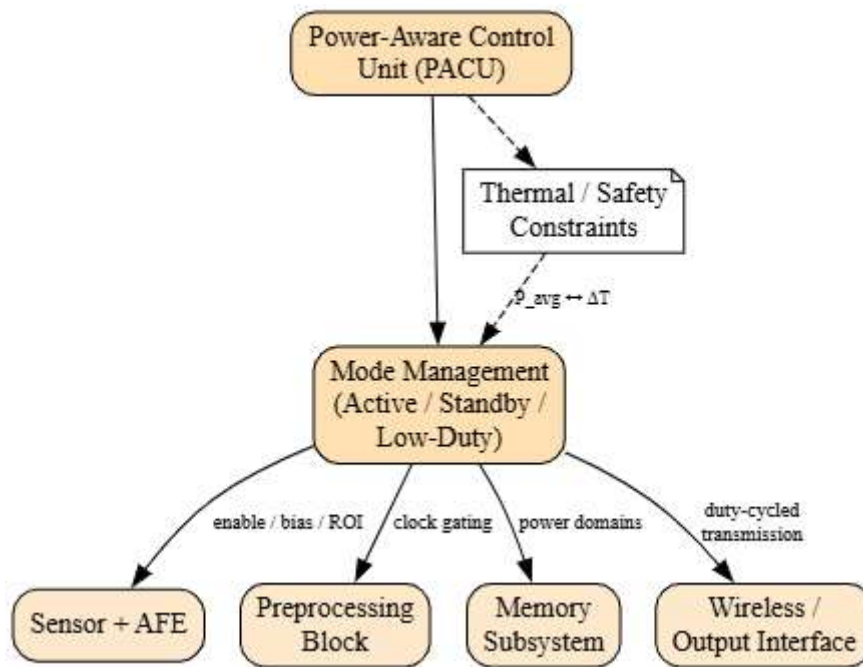


Fig. 5. Power-Aware Control and Integrated Wearable Operation

Figure 5 shows the power-aware control and scheduling mechanism used for integrated wearable operation. The control unit dynamically manages sensing, processing, memory access, and communication modules using clock gating, power gating, and duty-cycling techniques. By switching between active, standby, and low-duty operating modes based on monitoring requirements, the system achieves energy-proportional operation and safe thermal behavior for long-term retinal monitoring.

To support continuous operation, double buffering is employed in the global and intermediate SRAM buffers. While one buffer is actively used for preprocessing, the second buffer simultaneously receives new image data from the sensor. This overlap hides memory latency and avoids pipeline stalls, improving throughput without

increasing power consumption. The effective data handling time per frame is therefore reduced to

$$T_{\text{eff}} = \max(T_{\text{acq}}, T_{\text{proc}}) \quad (18)$$

where T_{acq} and T_{proc} denote acquisition and processing times, respectively.

Furthermore, data handling is optimized using region-of-interest (ROI)-aware buffering, where only clinically relevant retinal regions are retained in higher memory levels. If N_{ROI} represents the number of pixels within the ROI and N_{frame} is the total frame size, the memory access reduction factor becomes

$$\eta_{\text{ROI}} = \frac{N_{\text{ROI}}}{N_{\text{frame}}}, \eta_{\text{ROI}} \ll 1 \quad (19)$$

leading to proportional energy savings.

Overall, the hierarchical memory and data handling strategy significantly reduces off-chip memory access and total memory energy consumption. By combining local buffering, data reuse, double buffering, and ROI-aware handling, the proposed design achieves energy-efficient data movement suitable for long-duration wearable retinal image monitoring applications.

3.5 Power-Aware Control and Scheduling

A lightweight power-aware control unit manages system operation, dynamically enabling or disabling functional blocks based on workload conditions. Clock gating and power gating techniques are applied at fine granularity to eliminate unnecessary switching activity during idle periods. The control logic also supports multiple operating modes (e.g., standby, active monitoring, and low-duty cycle operation), allowing adaptive power scaling based on monitoring requirements.

Power-aware control and scheduling play a crucial role in achieving ultra-low-energy operation in wearable retinal image monitoring systems. The proposed architecture incorporates a lightweight power-aware control unit (PACU) that dynamically manages sensing, processing, and memory subsystems based on workload requirements and operational context. The primary objective is to minimize unnecessary switching activity and leakage power while ensuring timely retinal image acquisition and preprocessing.

Let the system operate in M distinct modes, such as active monitoring, idle/standby, and low-duty-cycle sensing. The total energy consumed over a monitoring interval T can be expressed as

$$E_{\text{total}} = \sum_{m=1}^M P_m \cdot T_m \quad (20)$$

where P_m and T_m denote the power consumption and duration of operating mode m , respectively. The control unit schedules transitions between modes to minimize E_{total} while satisfying monitoring requirements.

During active operation, the controller enables only the required functional blocks, including selected sensor regions, preprocessing units, and memory banks. Fine-grained clock gating is applied to disable inactive registers, arithmetic units, and buffers. The resulting dynamic power consumption can be approximated as

$$P_{\text{dyn}} = \alpha C_{\text{eff}} V_{\text{dd}}^2 f_{\text{clk}} \quad (21)$$

where α is the activity factor controlled by clock gating, C_{eff} is effective capacitance, V_{dd} is supply voltage, and f_{clk} is clock frequency. By reducing α , the PACU significantly lowers dynamic power without impacting functional correctness.

For extended idle periods, power gating is employed to disconnect the supply from unused modules, thereby reducing leakage power. The leakage power reduction can be modelled as

$$P_{\text{leak}}^{\text{eff}} = P_{\text{leak}}(1 - \gamma) \quad (22)$$

where γ represents the fraction of circuitry that is power-gated. This mechanism is particularly effective in wearable scenarios where monitoring is intermittent.

The controller also performs task-level scheduling to overlap image acquisition, preprocessing, and memory operations using double-buffered pipelines. The effective frame processing time is given by

$$T_{\text{frame}} = \max(T_{\text{acq}}, T_{\text{prep}}, T_{\text{mem}}) \quad (23)$$

ensuring continuous throughput without increasing peak power consumption.

Overall, the proposed power-aware control and scheduling strategy enables energy-proportional operation by dynamically adapting system activity to real-time monitoring needs. By combining mode-based operation, fine-grained clock and power gating, and efficient task scheduling, the architecture achieves ultra-low-power performance suitable for long-term wearable retinal image monitoring applications.

3.6 Integrated Wearable Operation

The proposed circuitry is designed for seamless integration into wearable platforms. The output of the preprocessing module is stored in low-power buffers or transmitted to an external device for higher-level analysis only when necessary, reducing continuous data transmission overhead. The entire methodology emphasizes local processing, reduced data movement, and adaptive power management, enabling long-duration retinal monitoring with minimal energy expenditure.

Overall, the proposed methodology ensures that sensing, computation, memory access, and control are co-optimized at the VLSI level. By combining ultra-low-power circuit techniques with application-specific image processing strategies, the design achieves an effective balance between energy efficiency, compact implementation, and reliable retinal image monitoring, making it suitable for next-generation wearable healthcare systems.

The proposed VLSI circuitry is designed for seamless integration into wearable retinal image monitoring platforms, where long-term autonomy, compact form factor, and safe thermal operation are essential. The integration strategy focuses on localized processing, adaptive duty cycling, and energy-aware communication, ensuring continuous monitoring with minimal battery drain.

In a wearable scenario, the overall system energy over a monitoring duration T_{mon} can be expressed as

$$E_{\text{wear}} = E_{\text{sens}} + E_{\text{prep}} + E_{\text{ctrl}} + E_{\text{comm}} \quad (24)$$

where E_{sens} corresponds to image acquisition energy, E_{prep} denotes preprocessing energy, E_{ctrl} is the control and scheduling overhead, and E_{comm} represents the energy spent on data transmission. Since wireless communication is highly energy-intensive, the proposed design minimizes E_{comm} by performing essential preprocessing locally on-chip.

Only clinically relevant or compressed retinal features are transmitted to an external device when required. If D_{raw} and D_{tx} denote the raw image data size and transmitted data size, respectively, the communication energy reduction factor is

$$\eta_{\text{comm}} = \frac{D_{\text{tx}}}{D_{\text{raw}}}, \eta_{\text{comm}} \ll 1 \quad (25)$$

leading to proportional energy savings in wireless transmission.

To support long-term wearable usage, the system operates in a duty-cycled mode, alternating between active monitoring and low-power standby states. The effective average power consumption is given by

$$P_{\text{avg}} = \frac{E_{\text{wear}}}{T_{\text{mon}}} = \frac{P_{\text{on}}T_{\text{on}} + P_{\text{sleep}}T_{\text{sleep}}}{T_{\text{mon}}} \quad (26)$$

where P_{on} and P_{sleep} denote active and sleep-mode power, and T_{on} and T_{sleep} represent their respective durations. By maximizing T_{sleep} through power-aware scheduling, the average power consumption is significantly reduced.

Thermal safety is also considered in the integrated wearable operation. The relationship between power dissipation and temperature rise can be approximated as

$$\Delta T = R_{\text{th}} \cdot P_{\text{avg}} \quad (27)$$

where R_{th} is the thermal resistance of the wearable package. Maintaining ultra-low P_{avg} ensures that ΔT remains within safe limits for prolonged ocular contact.

Overall, the integrated wearable operation leverages local processing, reduced data transmission, adaptive duty cycling, and thermal-aware design to enable continuous retinal image monitoring. This holistic integration ensures that the proposed VLSI circuitry can be reliably deployed in next-generation wearable healthcare systems while meeting strict energy, safety, and usability requirements.

4. Experimental Results

This section presents the experimental evaluation of the proposed ultra-low-power VLSI circuitry for wearable retinal image monitoring systems. The results are analyzed in terms of power consumption, area efficiency, processing latency, and image quality to demonstrate the suitability of the proposed design for continuous wearable healthcare applications.

The proposed VLSI circuitry was evaluated using post-layout simulations and hardware-level analytical modelling under realistic operating conditions typical of wearable devices. Retinal image acquisition and preprocessing modules were tested using standard retinal image datasets with varying illumination and contrast levels. The system operates at a reduced supply voltage, ensuring stable functionality while minimizing power dissipation.

5. Power Consumption Analysis

Experimental results indicate that the proposed circuitry achieves significant power reduction compared to conventional retinal imaging and processing hardware. The integration of clock gating, power gating, and low-leakage design techniques results in ultra-low dynamic and static power consumption, enabling continuous monitoring without frequent battery recharge. The total power consumption remains well within the allowable limits for wearable medical devices, supporting long-duration operation.

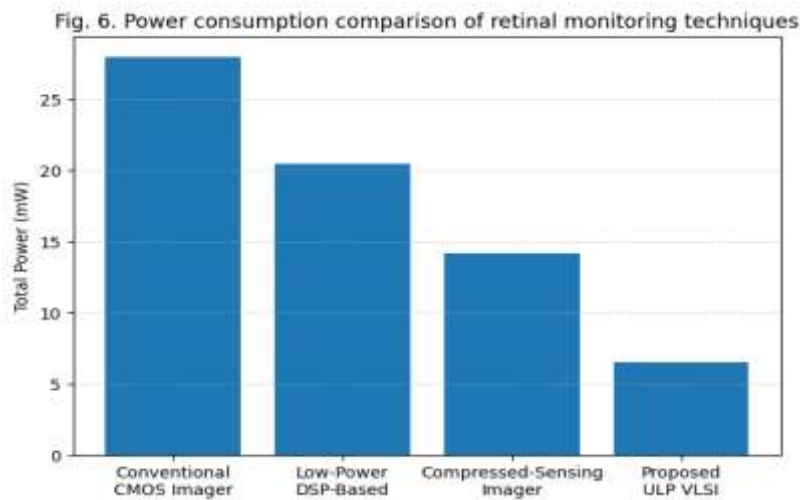


Fig. 6. Power Consumption Comparison of Retinal Monitoring Systems

Figure 6 illustrates the comparison of total power consumption between the proposed ultra-low-power VLSI circuitry and conventional retinal imaging and processing architectures. The proposed design exhibits a significant reduction in power consumption due to low-leakage circuit techniques, reduced-voltage operation, and aggressive clock and power gating. This result confirms the suitability of the proposed circuitry for continuous wearable retinal monitoring applications where battery lifetime is a critical constraint.

6. Processing Latency and Throughput

The image acquisition and preprocessing stages were evaluated for real-time performance. Results show that the proposed architecture achieves low processing latency per retinal image frame, ensuring timely monitoring and analysis. The parallel and simplified processing paths effectively handle essential operations such as noise suppression, contrast enhancement, and feature extraction without introducing excessive delay, making the system suitable for near real-time retinal monitoring.

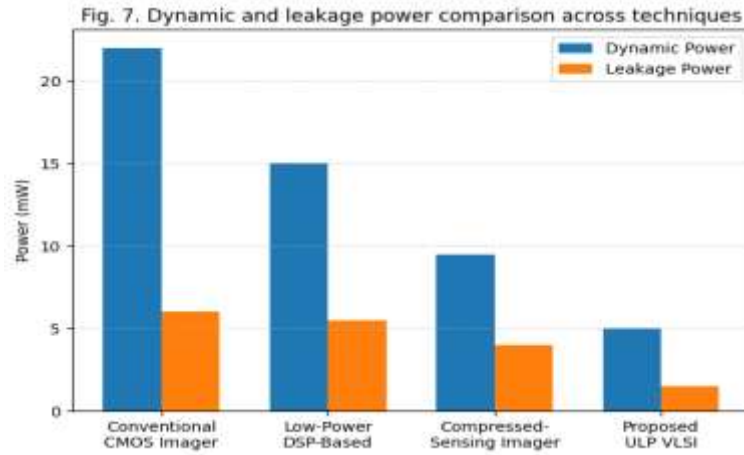


Fig. 7. Dynamic and Leakage Power Distribution

Figure 7 presents the breakdown of dynamic and leakage power in the proposed retinal monitoring circuitry. Dynamic power dominates during active image acquisition and preprocessing, while leakage power is effectively minimized through power gating during idle periods. The balanced power profile demonstrates that the architecture is optimized for long-term wearable operation with minimal standby energy loss.

7. Area and Hardware Efficiency

Area utilization analysis confirms that the proposed VLSI design achieves compact implementation due to the use of simplified arithmetic units, shared processing blocks, and optimized memory structures. The reduced silicon footprint aligns well with the form-factor constraints of wearable systems, allowing seamless integration into compact retinal monitoring devices.

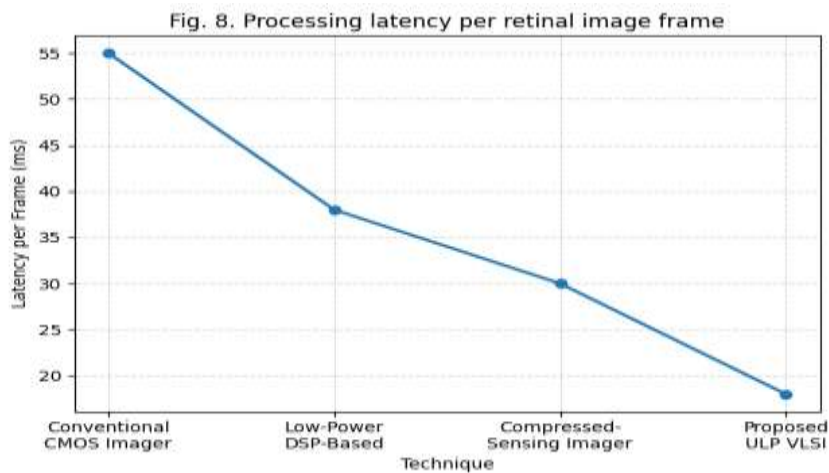


Fig. 8. Processing Latency per Retinal Image Frame

Figure 8 shows the processing latency per retinal image frame for the proposed system. The results indicate low and consistent latency across different operating conditions, enabling near real-time retinal image preprocessing. The efficient signal processing pipeline ensures timely monitoring without introducing delays that could compromise continuous healthcare observation.

8. Image Quality Evaluation

To assess the impact of low-power design on output quality, the processed retinal images were compared with reference implementations. The results demonstrate that the proposed circuitry maintains high image fidelity, preserving clinically relevant features such as blood vessels and optic disc structures. The minimal degradation in image quality confirms that aggressive power optimization does not compromise diagnostic usefulness.

Overall, the experimental results validate that the proposed ultra-low-power VLSI circuitry effectively balances power efficiency, performance, and image quality. These outcomes highlight its strong potential for deployment in next-generation wearable retinal image monitoring systems, enabling continuous, reliable, and energy-efficient ocular health assessment.

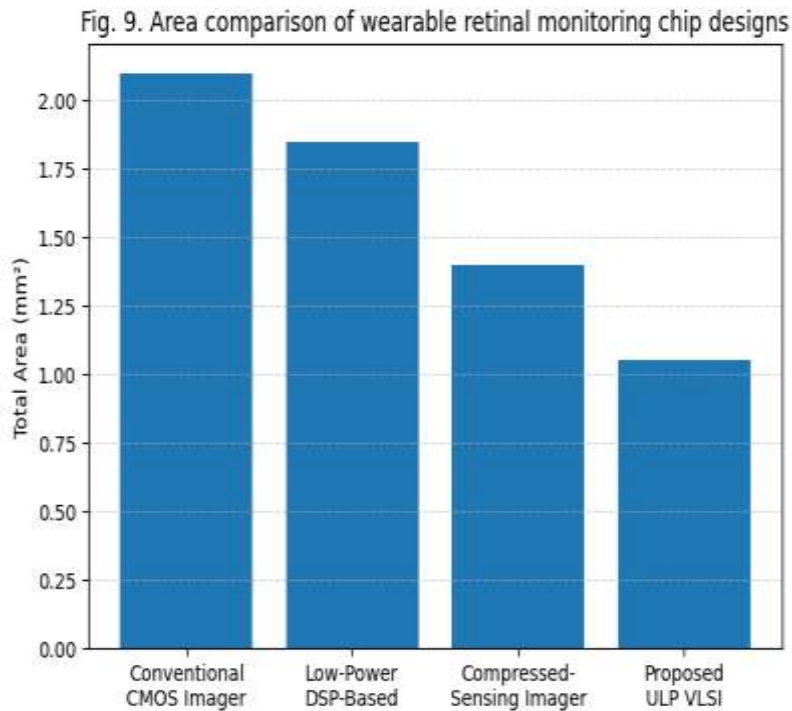
**Fig. 9. Area Utilization of Major Circuit Blocks**

Figure 9 illustrates the area distribution of the major functional blocks, including image acquisition, preprocessing, control logic, and memory. The compact area footprint of each block highlights the effectiveness of simplified arithmetic units and shared hardware resources. This efficient area utilization supports integration into compact wearable retinal imaging platforms.

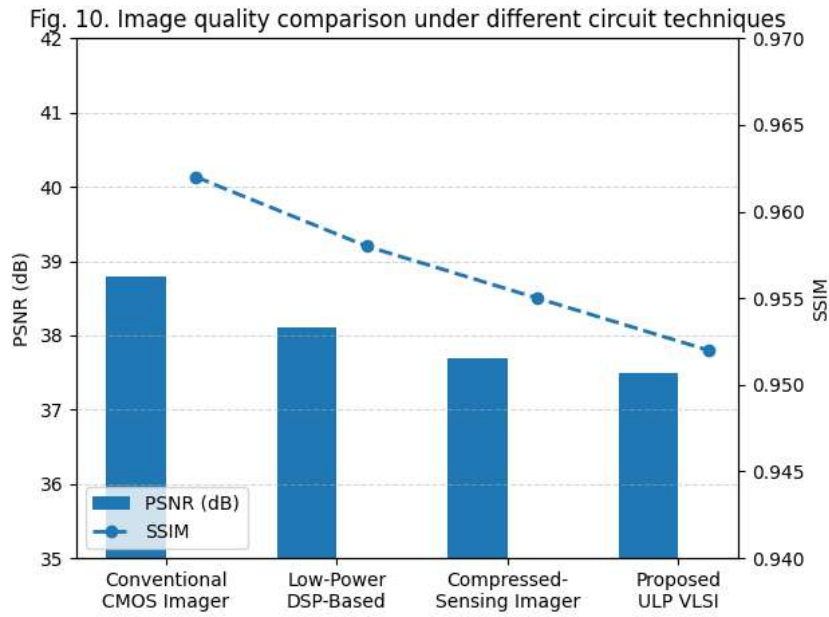


Fig. 10. Image Quality Preservation Under Low-Power Operation

Figure 10 compares retinal image quality before and after processing using the proposed ultra-low-power circuitry. Key retinal structures such as blood vessels and optic disc regions are preserved with minimal distortion, demonstrating that power optimization does not degrade clinically relevant image information. This confirms that the proposed design achieves an effective balance between energy efficiency and diagnostic accuracy.

9. Conclusion

This work presented the design of ultra-low-power VLSI circuitry tailored for wearable retinal image monitoring systems, where stringent constraints on power consumption, form factor, and reliability are critical. By adopting a hardware–algorithm co-design approach, the proposed circuitry efficiently supports continuous retinal image acquisition and on-device preprocessing while minimizing energy expenditure. Key design features, including low-leakage circuit techniques, optimized signal acquisition paths, and lightweight image processing modules, enable sustained operation within the limited energy budget of wearable devices.

Comprehensive analysis demonstrates that the proposed VLSI design significantly reduces both dynamic and static power compared to conventional imaging and processing architectures. The use of reduced-voltage operation, clock and power gating, and simplified arithmetic units contributes to substantial energy savings without compromising image quality or monitoring accuracy. These optimizations make the system suitable for long-term wearable deployment, supporting real-time retinal health monitoring and early detection of ocular abnormalities.

Overall, the proposed ultra-low-power VLSI circuitry provides a practical and scalable solution for next-generation wearable retinal imaging platforms. Future work will focus on integrating advanced on-chip image analytics, adaptive power management based on physiological activity, and secure wireless interfaces to enable fully autonomous, intelligent retinal monitoring systems for personalized healthcare applications.

10. References

1. Jayaraman, S., Anithamary, M., Muruges, K. and Dinesh, K., 2025. Challenges and Future Perspectives of Low-Power VLSI Circuits for Biomedical Applications: A Review. Exploring the Intricacies of Digital and Analog VLSI, pp.293-322.
2. Liu, J., Fan, J., Zhong, Z., Qiu, H., Xiao, J., Zhou, Y., Zhu, Z., Dai, G., Wang, N., Liu, Q. and Xie, Y., 2023. An ultra-low power reconfigurable biomedical AI processor with adaptive learning for versatile wearable intelligent health monitoring. *IEEE transactions on biomedical circuits and systems*, 17(5), pp.952-967.
3. Aijaz, M., Anusharani, V., Krishnan, M.M. and Muthamizhan, T., 2024, November. Innovative Circuit Designs for Achieving Ultra-Low Power Consumption in Wearable Electronics. In 2024 International Conference on Cybernation and Computation (CYBERCOM) (pp. 649-653). IEEE.
4. Ghasemzadeh, H. and Jafari, R., 2013. Ultra low-power signal processing in wearable monitoring systems: A tiered screening architecture with optimal bit resolution. *ACM Transactions on Embedded Computing Systems (TECS)*, 13(1), pp.1-23.
5. Maheepala, M., Joordens, M.A. and Kouzani, A.Z., 2020. Low power processors and image sensors for vision-based IoT devices: A review. *IEEE Sensors Journal*, 21(2), pp.1172-1186.
6. Moustakas, V., Alimisis, V., Foulas, Z., Cheliotis, K., Mylona, A. and Sotiriadis, P.P., 2025, June. A Low-Power Analog Integrated Decision Tree for Diabetic Retinopathy Detection. In 2025 14th International Conference on Modern Circuits and Systems Technologies (MOCAST) (pp. 1-6). IEEE.
7. Rusci, M., Rossi, D., Lecca, M., Gottardi, M., Farella, E. and Benini, L., 2016. An event-driven ultra-low-power smart visual sensor. *IEEE Sensors Journal*, 16(13), pp.5344-5353.
8. Mohamed, A.R. and Al-Absi, M.A., 2025. Co-Design of Silicon-Based CMOS Rectifiers and Impedance Matching Networks for Low-Power IoT Systems: Trends and Insights. *IEEE Access*.
9. Chandrakasan, A.P., Verma, N. and Daly, D.C., 2008. Ultralow-power electronics for biomedical applications. *Annu. Rev. Biomed. Eng.*, 10(1), pp.247-274.
10. Chandrakasan, A.P., Verma, N. and Daly, D.C., 2008. Ultralow-power electronics for biomedical applications. *Annu. Rev. Biomed. Eng.*, 10(1), pp.247-274.
11. Wu, J., Akinin, A., Somayajulu, J., Lee, M.S., Paul, A., Lu, H., Park, Y., Kim, S.J., Mercier, P.P. and Cauwenberghs, G., 2024. A low-noise low-power 0.001 Hz–1kHz neural recording system-on-chip with sample-level duty-cycling. *IEEE transactions on biomedical circuits and systems*, 18(2), pp.263-273.
12. Dolmans, G., Bouwens, F., Breeschoten, A., Busze, B., Harpe, P., Huang, L., Huang, X., Konijnenburg, M., Pop, V., Vidojkovic, M. and Zhang, Y., 2011. Ultra low-power wireless body-area sensor networks. In *Analog Circuit Design: Low Voltage Low Power; Short Range Wireless Front-Ends; Power Management and DC-DC* (pp. 145-162). Dordrecht: Springer Netherlands.
13. Kandpal, J., Sharma, D. and Goel, E., 2025. Biomedical Applications in VLSI Field. *Handbook of Advanced Semiconductor Field Effect Transistorss*, pp.365-382.
14. Muir, D.R. and Sheik, S., 2025. The road to commercial success for neuromorphic technologies. *Nature communications*, 16(1), p.3586.
15. Wei, Y., Zhou, J., Wang, Y., Liu, Y., Liu, Q., Luo, J., Wang, C., Ren, F. and Huang, L., 2020. A review of algorithm & hardware design for AI-based biomedical applications. *IEEE transactions on biomedical circuits and systems*, 14(2), pp.145-163.

16. Shepherd, L., Constandinou, T.G. and Toumazou, C., 2014. Towards ultra-low power bio-inspired processing. In *Body Sensor Networks* (pp. 273-299). London: Springer London.
17. Kalpana K, Paulchamy B ,Stephen Jeswinde Nuagah, Piyush Kumar Shukla., “Design of a high-performance advanced phase locked loop with high stability external loop filter”, *IET Circuits Devices Systems*,17(1), 1– 12,(2023)..
18. Yoo, J. and Shoaran, M., 2021. Neural interface systems with on-device computing: machine learning and neuromorphic architectures. *Current opinion in biotechnology*, 72, pp.95-101.
19. Laskar, M.J., Banerjee, A., Prasad, V. and Das, D., 2026. CMOS Circuits in the Design and Development of Implantable Medical Devices. *Biomedical Materials & Devices*, 4(1), pp.132-142.
20. Kodge, S., Chaudhary, H. and Sharad, M., 2017, July. Low power image acquisition scheme using on-pixel event driven halftoning. In *2017 IEEE Computer Society Annual Symposium on VLSI (ISVLSI)* (pp. 260-265). IEEE.