

## **QCA DESIGN FOR 4-BIT ASYNCHRONOUS DOWN COUNTER**

Dr. Thivya K.S,  
Department of Electronics and Communication Engineering,  
Easwari Engineering College,  
Chennai, India  
*thivya.grassdew@gmail.com*

Anandhi S,  
Department of Electronics and Communication Engineering,  
Dr. M.G.R Educational and Research Institute,  
Chennai, India  
*anandhibalaji04@gmail.com*

Sudhaman K,  
Department of Electronics and Communication Engineering,  
Dr. M.G.R Educational and Research Institute,  
Chennai, India  
*sudhaman.ece@drmgrdu.ac.in*

**Abstract:** Quantum Cellular Automata (QCA) is a transistor-less computation model that addresses the problem of device interconnection and density which holds the promise of high speed and fewer sizes compare to the Complementary Metal Oxide Semiconductor (CMOS) design. In this study, the design of 4-bit down asynchronous counter which is the fundamental block of the digital technology using new D-Flip Flops (D-FF) layouts is discussed. This D-FF is designed using majority gates. The FF clock inputs are not driven by the same clock and each FF output depends on the previous output. This design finds its application in nanotechnology fields including medical field to monitor the patient's activity by utilizing timer based tools. The design of 4-bit down asynchronous counter is simulated in the QCA design tool.

**Keywords:** QCA, Asynchronous counter, D Flip-flop, majority gate

### **I. INTRODUCTION**

QCA systems consist of arrays of interacting cells. Each cell affects its neighbors and it is possible to propagate information and compute logic functions without physical signal propagation. Another application of crossing minimization algorithms is QCA. The non-adiabatic switching power and polarization error in QCA design circuits is estimated in [1] using a probabilistic modeling tool. A full adder is designed in [2] to enhance the switching level at nanoscale level with the help of high level synthesis. A QCA model is designed in [3] using majority gates and also the model is employed in various parallel prefix adder.

The 2 bit, 3 bit and 4 bit binary to gray converter is described in [4] to analyze the area, power and switching speed occupied by the designed circuit. A 2:1 and 4:1 MUX design of QCA model is designed in [5] to minimize the area and cell count. The QCA full adder with high performance in [6] is used in ripple carry adder which reduces the cell number compare to the other adders. The defect tolerance of circuits and sequential devices implemented by molecular QCA is described in [7] and also defects of logic level characterization is studied in the simulation results.

A unique timing constraint is investigated in [8] for Reset-Set FF and D-FF QCA model. For designing FFs, positive level triggered and falling edge triggered approach are employed in [9] using T-FF for N-bit which offers less power. An XOR gate with 2, 4 and 8-input is designed by utilizing QCA model in [10]. It offers less complexity than existing XOR gates. A hybrid full adder is described in [11] using CMOS design and achieved high speed and low power. A reversible multiplier is designed in [12] using CMOS design. It offers less power dissipation.

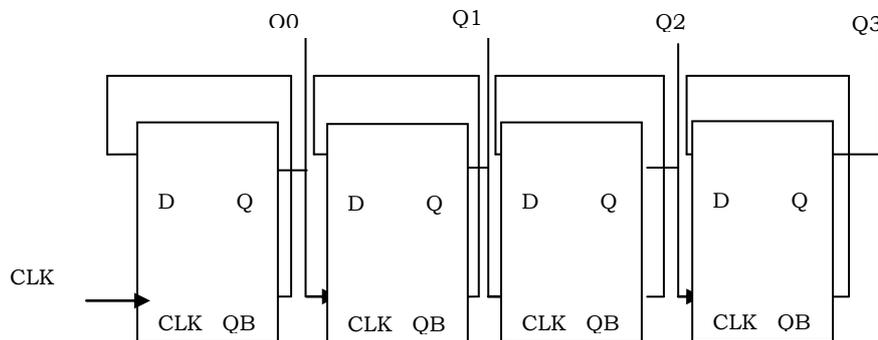
D latch, T-FF, D-FF, SR latch, 4-bit T-FF register, 2-bit counter are designed in [13] with low power and sizes. A synchronous counter using D-FF QCA is described in [14] which achieves efficient and robust. A reversible 2X2 crossbar switch is designed in [15] which is suitable for low power application.

The literature survey shows that many researchers introduced different approach for crossing minimization through routing and partitioning. Their results are aimed to produce the calculation uniquely as well as advanced design by QCA. The objective of this work is to explore the new approach with less complication in asynchronous design. Further, the paper is organized by the proposed design in section 2, simulation results in section 3 and conclusion in section 4.

## **II. METHODS AND MATERIALS**

The output which depends on the past output and present input is referred as FF which stores 1 bit information 1 or 0. By an external clock only the first FF is clocked. Then, by the output of the proceedings FF, all subsequent FF are clocked. The reverse operation of the up counter is the down counter. The pulse transmission delay from the FF to FF in the asynchronous counter is high than synchronous counter which causes slower speed.

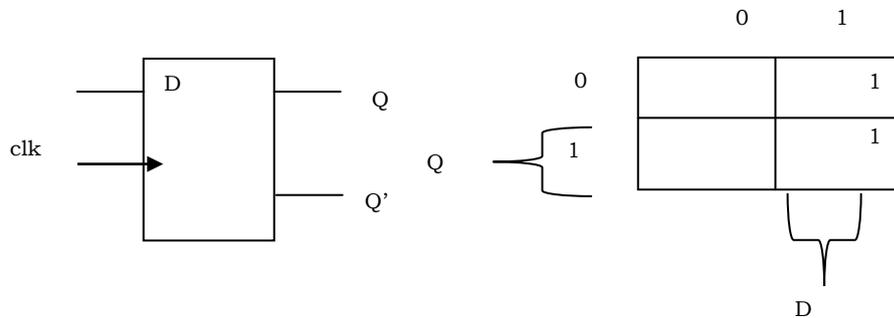
The clock pulse ripples through FF so the asynchronous counter is also named as ripple counters. Figure 1 shows the 4-bit asynchronous counter which is a simple modification of the UP counter. From 15 to 0 downwards, the 4 bit down counter will counts the numbers.



**Fig. 1 4-bit Down Asynchronous counter**

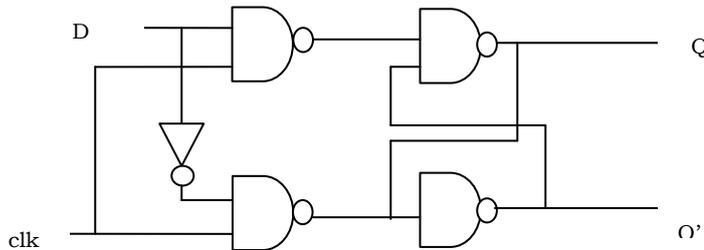
The input D of all FF are linked to logic '1' and the input clock of all FFs are cascaded. At every positive edge clock signal the FF will toggles. The input clock is connected to the first FF. The other FF receives the input clock signal from pervious FF output Q in the counter rather than output Q. In the 4-bit down counter Q0, Q1, Q2, Q3 stands for count which is shown in the Fig. 1. If the active

edge clock signal takes place then the output of first FF is changed. For instance the current count is 2 then the down counter will compute the next count as 1. The clock input is the origin of variation in the next FF output count. For each clock pulse at the input will decrease the each FF count. Thus the down counter counts from 15, 14, 13...0. Figure 2 (a) and (b) depicts the D-FF symbol and its characteristics equation generation respectively. The characteristic equation for D-FF is  $Q(t+1) = D$  and with the help of this equation the FF are designed using QCA binary wires.



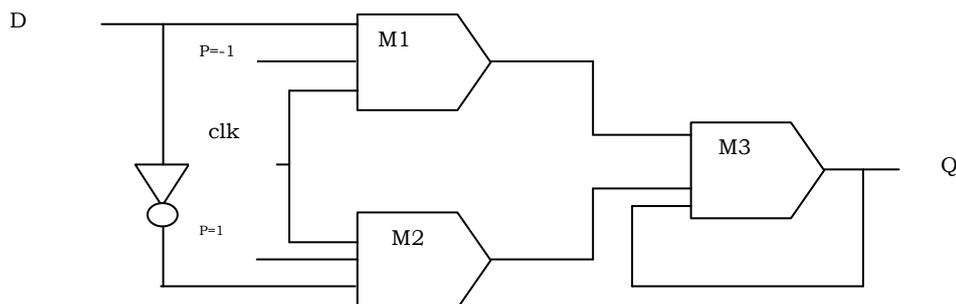
**Figure 2 (a) D-FF (b) Generating characteristic equation**

Figure 3 illustrates the logic diagram of the D-FF. When the input CP is ON the binary information at the input will shifted to output Q.



**Fig.3 Basic logic diagram of the D FF**

The output follows the input data when the pulse remains in its state 1. Figure 4 shows the D-FF design using majority gates. Here M1 is AND gate, M2 is OR gate and M3 acts as OR gate.

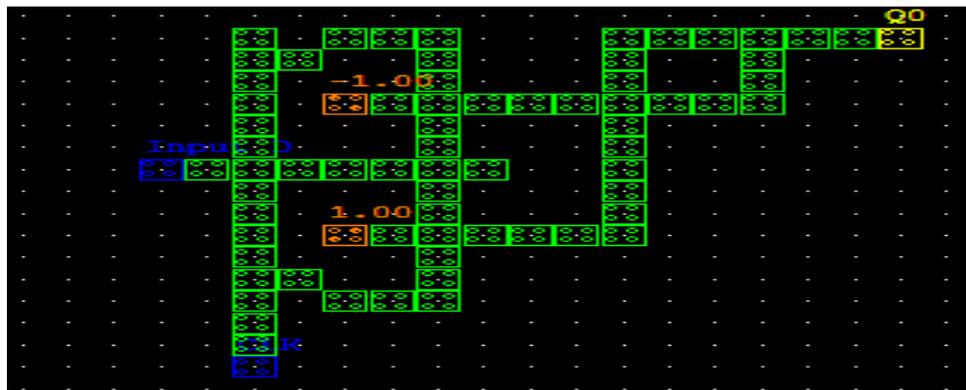


**Fig.4 D-FF using Majority gates**

In Fig. 4,  $P$  represents polarization. If  $P=-1$  symbolize the logic 0 and  $P=+1$  symbolize the logic 1 binary information.

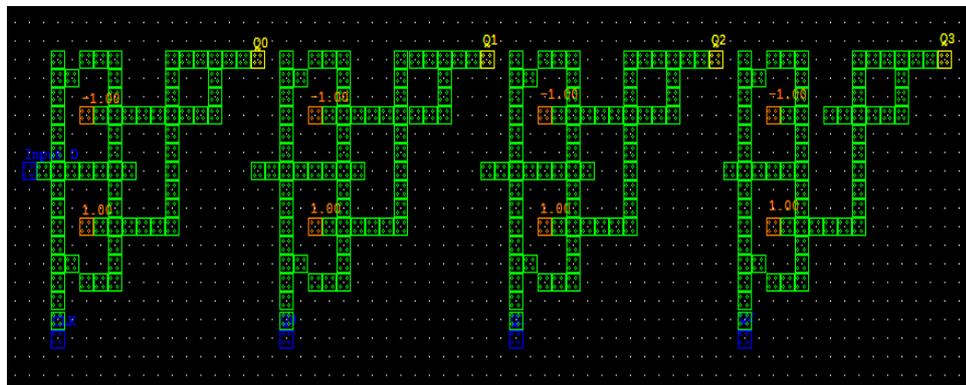
### III. RESULTS AND DISCUSSION

The design of QCA model is different from the conventional CMOS design model due to their clocking approaches. The 4-bit asynchronous down counter using D-FF is designed using QCA design tool. Figure 5 shows the layout of QCA design using D-FF by majority gate.



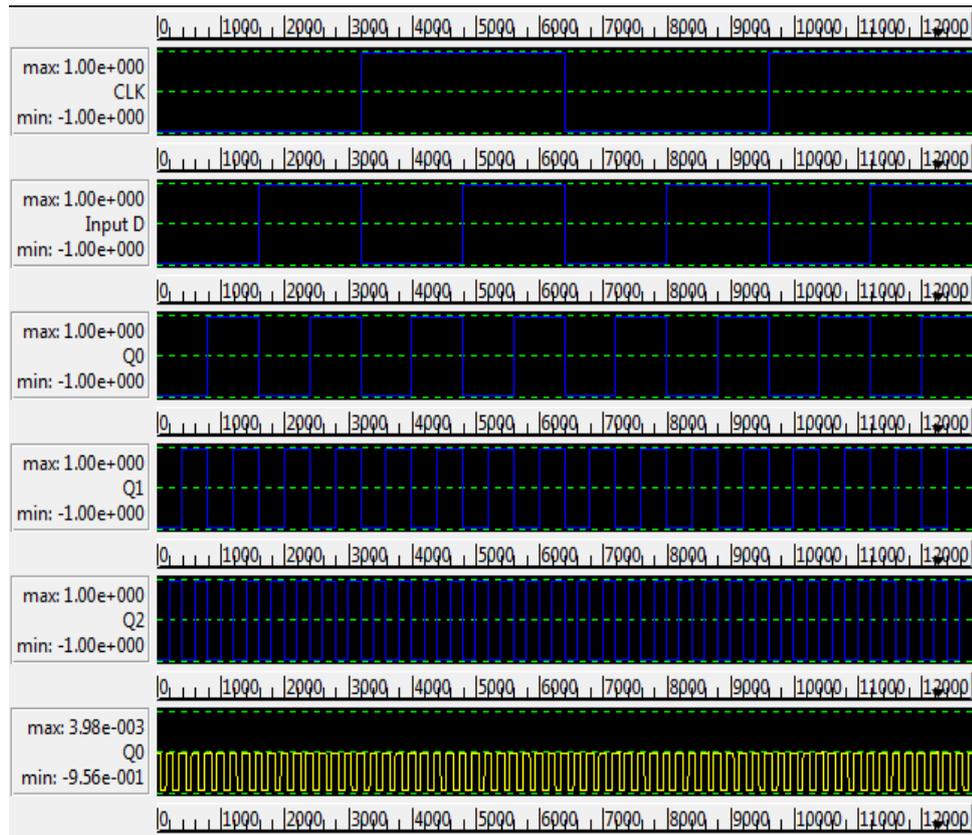
**Figure 5 D FF Layout using Majority gates**

This layout has one control clock and one input D. In this layout D is the input CLK is the clock input Q0m is the output.69 cells are required for this realization. The 4-bit down asynchronous counter design is shown in Fig. 6.It is constructed using D-FF.



**Figure 6 Layout of the 4-bit Asynchronous down counter using D FF**

It is a 4-bit counter so it has 4 D-FF. In order to perform the operation of the asynchronous counter it requires 276 cells. The input-output delay of this design is based on the each FF output. Figure 7 shows the simulation waveform for the 4 bit asynchronous counter using new D-FF layouts.



**Figure 7 Simulation waveform of 4-bit asynchronous counter using D-FF**

In the waveform each input clock pulse will decrease the count of each FF. Thus the down counter counts from 15, 14, 13...0. Here *clk* and *D* are the input waveforms, whereas *Q0*, *Q1*, *Q2*, *Q3* are the output waveforms. The output *Q1* depends on the input *clk* and *D*, but the output of for *Q2*, *Q3*, *Q4* depend on its previous FF output.

#### IV. CONCLUSION

In this study, 4-bit asynchronous down counter using new D-FF layouts are realized in QCA technology. It can be used in any nano-scale applications with less complex cell design. The functionality and layouts are implemented using the QCA design software tool for 4-bit asynchronous counter. This QCA design models are smaller than the CMOS technology. Here the D-FF is constructed using majority gates with one control input clock. The output of one FF is represented as a clock of consecutive FF in asynchronous counter design. With the help of QCA clock, the correct flow of data information is maintained using QCA wire. In future, the work is extended to dual edge triggered structure based 4-bit asynchronous counter.

## **REFERENCES**

- [1]. S. Srivastava, A. Asthana, S. Bhanja, and S. Sarkar, "QCA Pro-an error-power estimation tool for QCA circuit design", IEEE international symposium of circuits and systems, 2011, pp. 2377-2380.
- [2]. A. Roohi, R.F. DeMara, and N. Khoshavi, "Design and evaluation of an ultra-area-efficient fault-tolerant QCA full adder", Microelectronics Journal, Vol.46, No.6, 2015, pp.531-542.
- [3]. V. Pudi, and K. Sridharan,"Low complexity design of ripple carry and Brent-Kung adders in QCA", IEEE Transactions on nanotechnology, Vol.11,No.1, 2015, pp.105-119.
- [4]. M. Abdullah-Al-Shafi, and A.N. Bahar, "Novel binary to gray code converters in QCA with power dissipation analysis," International journal of multimedia and ubiquitous engineering, Vol. 11, No. 8, 2016, pp.379-396.
- [5]. A. Tambe, S. Bhakre, and S. Kassa, "Design and Analysis of (2x1) and (4x1) Multiplexer Circuit in Quantum dot Cellular Automata Approach", International Journal of Innovative Technology and Exploring Engineering, Vol.8, No.6S3, 2011, pp.227-281.
- [6]. M. Mohammadi, M. Mohammadi, and S. Gorgin," An efficient design of full adder in quantum-dot cellular automata (QCA) technology", Microelectronics journal, Vol.50, 2016, pp.35-43.
- [7]. M. Momenzadeh, J. Huang, and F. Lombardi, "Defect characterization and tolerance of QCA sequential devices and circuits", IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems, 2005, pp. 199-207.
- [8]. J. Huang, M. Momenzadeh, and F. Lombardi, "Design of sequential circuits by quantum-dot cellular automata". Microelectronics Journal, 38(4-5), 2007, pp.525-537.
- [9]. S. Pandey, S. Singh, and S. Wairya," Designing an efficient approach for JK and T flip-flop with power dissipation analysis using QCA", International Journal of VLSI design & Communication Systems Vol.7, No.3, 2016 pp.29-48.
- [10]. R. Laajimi, A. Ajimi, L. Touil, and A.N. Bahar, "A Novel Design for XOR Gate used for Quantum-Dot Cellular Automata (QCA) to Create a Revolution in Nanotechnology Structure", International Journal of Advanced Computer Science and Applications, Vol. 8,No.10, 2017, pp.279-287.
- [11]. K. Maheshwaran, "CMOS Design of Low Power High Speed Hybrid Full Adder", International Journal of MC Square Scientific Research, Vol.8, No.1, 2016, pp.16-22.
- [12]. S. Alexander, "Design And Implementation Of Efficient Reversible Multiplier Using Tanner Eda", International Journal of MC Square Scientific Research, Vol.5, No.1, 2013, pp-15-22.
- [13]. A. Swapna, and A. Hariprasad, "Design of Sequential Circuit Using Quantum-Dot Cellular Automata (QCA)", International Journal of Advanced Engineering Research and Science, Vol. 3,No.9, 2016, pp.95-100.
- [14]. M.M. Abutaleb, "Robust and efficient quantum-dot cellular automata synchronous counters", Microelectronics Journal, Vol. 61, 2017, pp.6-14.
- [15]. J.C. Das, and D. De, "Nanocommunication network design using QCA reversible crossbar switch", Nano communication networks, Vol.13, 2017, pp.20-33.