SERIAL ADDER BASED MULTIPLICATION AND ACCUMULATION UNIT (MAC)

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Abstract: For efficient digital FIR filter applications, the Multiplication and Accumulation (MAC) unit is implemented by using various methods. In a digital filter, the MAC unit is one of the main units for performing multiplications and additions. This paper presents an efficient filter design for digital signal processing (DSP) applications with the reduction of carry propagation. In general, the performance of transpose filter mainly depends on the design of MAC unit. The design of a traditional filter consists of a large number of logical elements and has a high computational delay due to the conventional MAC unit. To design an efficient MAC unit, a serial adder is employed by using 2:1 multiplexer and a shifter block. The proposed work is implemented by using Xilinx ISE synthesis tool.

Keywords: Finite Impulse Response (FIR) Filter, Adder, Multiplier, Multiplication and Accumulation (MAC) Unit, Multiplexer, Digital Signal Processing (DSP).

I. INTRODUCTION

Tri-state logic based Infinite Impulse Response (IIR) and Finite Impulse Response (FIR) filter implementation are discussed in [1]. The extensibility and modularity of tri-state logic are also outlined. It uses the following concepts such as pipelining, tri-state logic, and parallel operation for the filter implementation. The circuit complexity is reduced due to the tri-state logic in the design. The shared concept of multipliers is extended so that the throughput speed is increased along with the parallel operation of multiplication.

A simple first order filter with multiple outputs is designed in [2] which require only four adders and a delay and multiplier unit. It eliminates the forced overflow oscillations, constant and zero input. Due to its simple structure, it is mainly used in VLSI implementation.

A decimation filter is designed in [3] for use in delta-sigma coder. It is a FIR low pass filter with 20-bit internal width and clock frequency of 15.36 MHz. The design consists of a cascade structure of FIR and IIR filters. The former one uses four taps transversal filter with serial in parallel out structure, and the later one uses three recursive filters of first order connected serially. It is a part of analog to digital converter and employed in an echo cancelling system.

A non-recursive digital filter is designed in [4] using fixed point binary coefficient. The complexity of such a design depends on the number of adders used in the multiplier section. The complexity of standard binary representation is

reduced by using Canonic Signed Digit (CSD) representation. It requires fewer adders than Bull and Horrocks algorithm. The reduced added graph algorithm has two parts; optimal and heuristic. In the former step, the adder cost is minimized.

A hardware optimization is discussed in [5] using CSD representation. It determines the minimum order filter at first by assuming that the filter coefficients are infinite precision. Then, the filter order is increased by truncating the filter coefficients. An easy approach for FIR filter design is described in [6] using a minimum number of filter coefficients. The filter coefficients are obtained from the value of sampling function which has singular points. In comparison with Remez method, it requires a minimum number of filter coefficients.

An approach to reduce the complexity of parallel FIR filter is discussed in [7]. It uses linear and iterated short convolution techniques. The structure of parallel FIR filter is removed by using liner convolution structure which reduces the hardware cost. A transpose structure is designed in [8] to reduce the complexity of fixed point FIR filters. A minimum spanning tree approach is used to design a multiplier blocks. Fixed points filter coefficients are partitioned into sub-sets to reduce the complexity of FIR filter in [9].

In this paper, an efficient filter design with the reduction of carry propagation is presented. The following sections give the overview of FIR design with serial adder and their performance in terms of number of slices, Look Up Table (LUT), and delay.

II. FINITE IMPULSE RESPONSE FILTER BASED SERIAL ADDER

The proposed digital FIR Filter is implemented by using serial adder. The adder is one of the important units for performing multiplication and accumulation. In order to construct an eight-bit serial adder, one-half adder and seven full adders are required. Serial adders are used to reduce the computational delay, and also some logical elements count. It is used to perform bit by bit additions with efficient area utilizations. In a serial adder block, two single bit inputs are available in order to determine the carry out signal. Figure 1 shows the traditional multiplexer based multiplier unit.

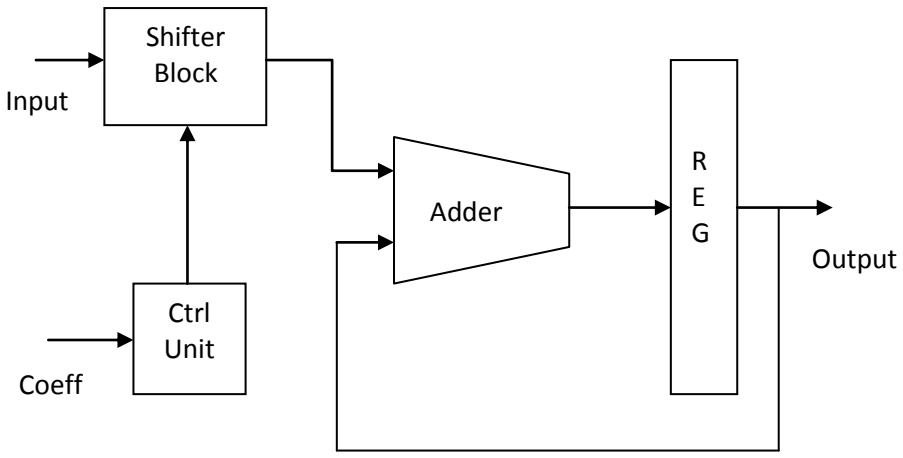

Fig. 1 Traditional multiplexer based multiplier unit

The multiplier structure consumes more area than multiplexer based structure. The operation of multiplexer depends on the control signal value. The diagram of a shifter block exposed in Figure 1 has 8-bit vector for inputs. The output is a shifted version of the input and the quantity of shift depends on the control signal value. The shifting operation in the input signal is controlled by the barrel shift register that uses only combinatorial logic. The control signal provides the number of shift to the barrel shifter. Figure 2 shows the architecture for the serial adder for MAC unit.

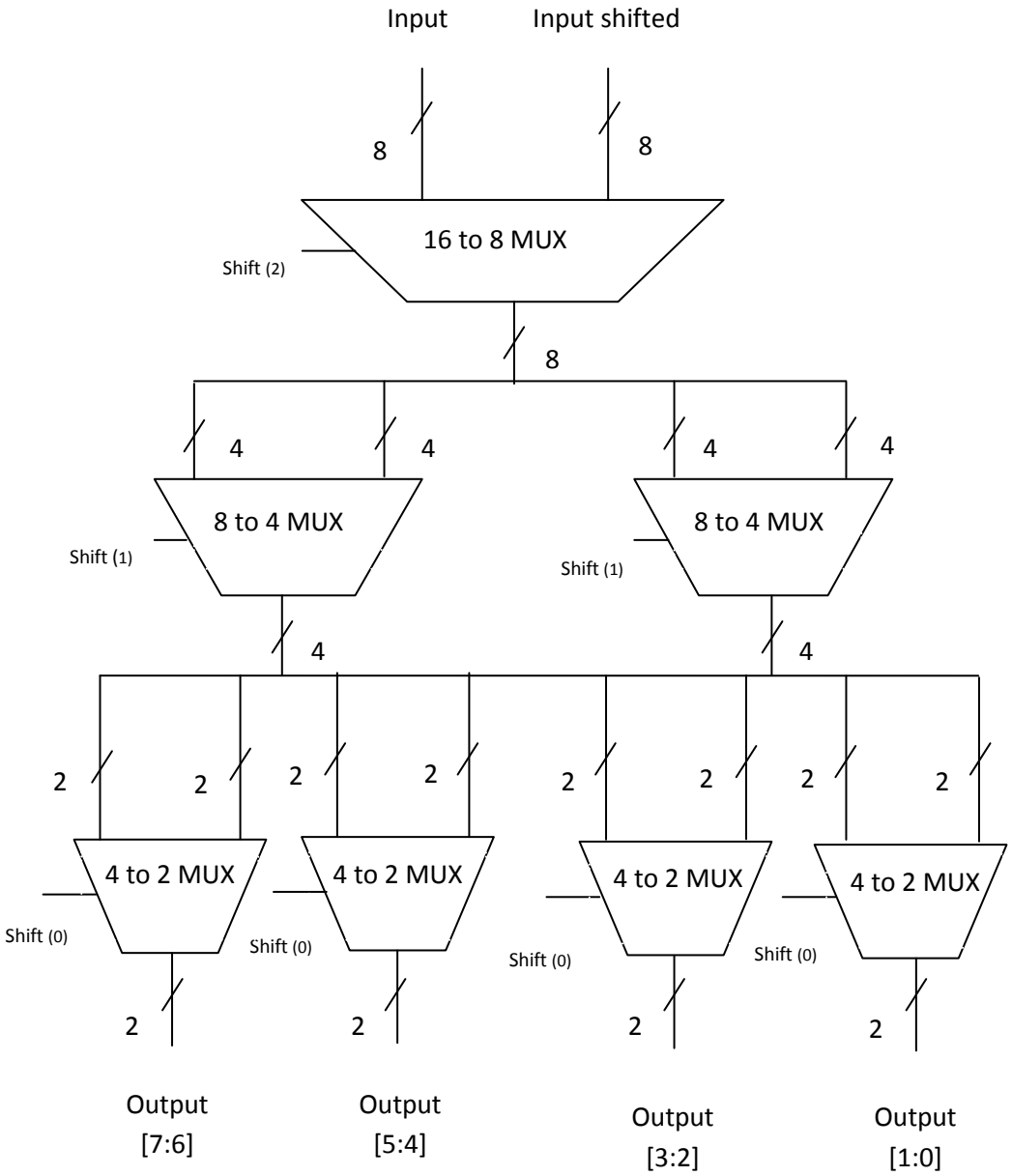

Fig. 2 Architecture for the serial adder for MAC unit

III. RESULTS AND DISCUSSION

The proposed serial adder is implemented by using Verilog Hardware Description Language (HDL).The simulation results are evaluated by using Modelsim XE and the synthesis is estimated by using the Xilinx ISE software. Table 1 shows a comparison of adder circuits. Figure 3 shows the simulation result for the FIR filter based serial adder and Figure 4 shows the graphical representation of synthesis results. Results show that the numbers of logical elements and the computational delay are highly reduced than the traditional method. The conventional multiplexer based multiplier unit requires a high number of logical elements counts.

TABLE 1 Comparison of Adder circuits

Description	Slices	LUT	Delay (ns)
Traditional FIR filter based multiplexer based adder	21	41	35.376
Proposed FIR Filter based serial adder	20	40	28.222

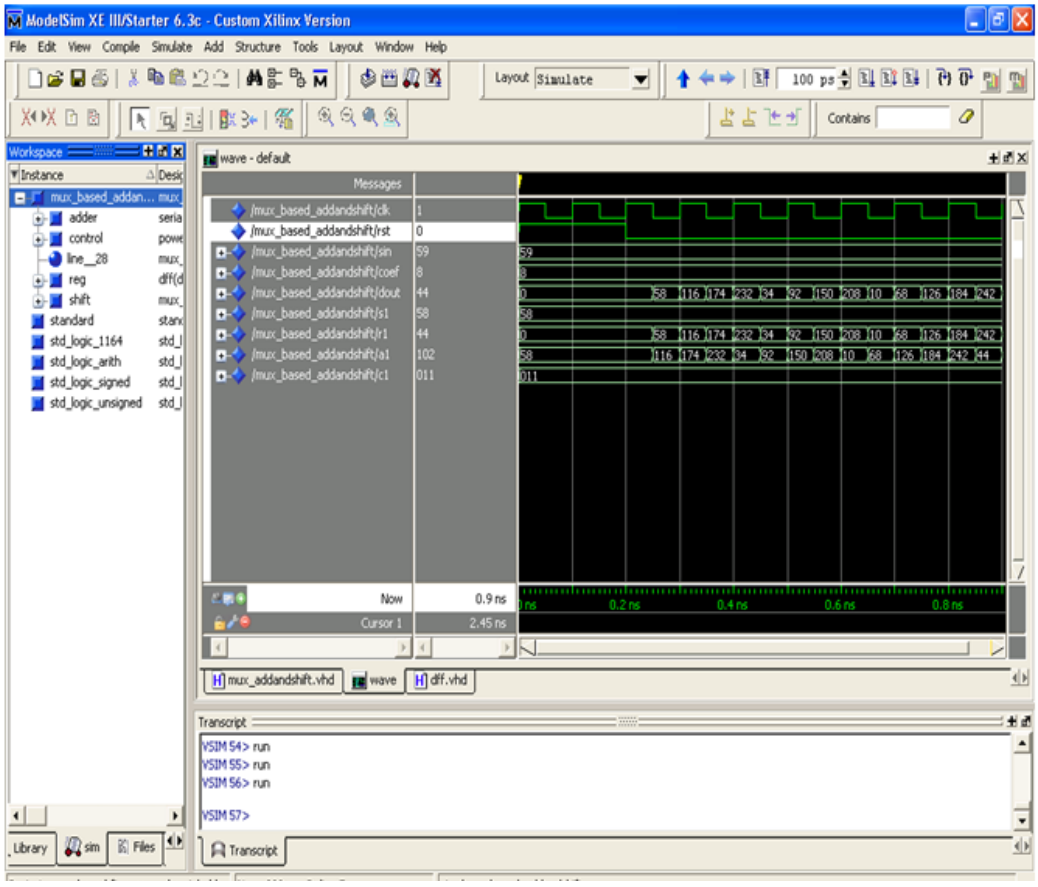

Fig. 3 Simulation result for the FIR Filter based Serial Adder

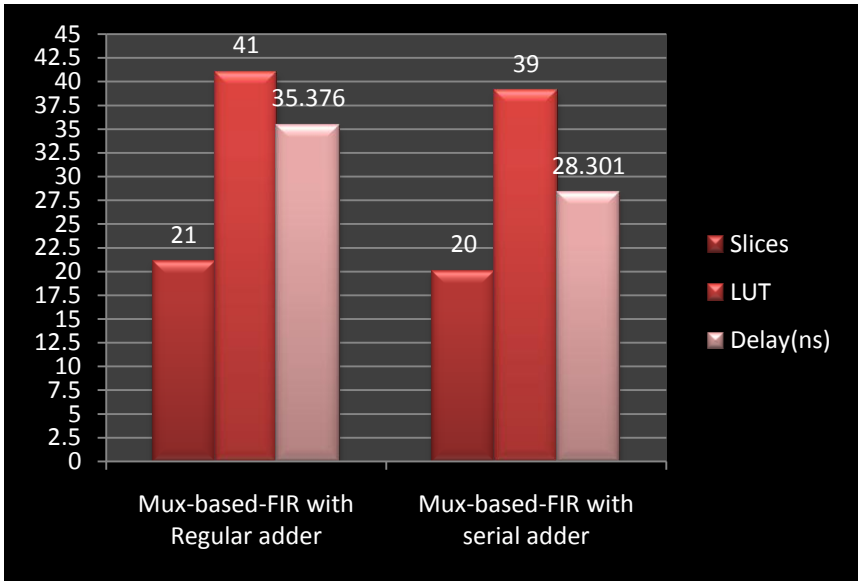

Fig. 4 Graphical representation for synthesis results

IV. CONCLUSION

In this paper, a control based shift and move based serial adder is presented. This strategy is utilized for advanced FIR channel outline and execution. This strategy utilizes serial adder design for the construction. It makes the channel coefficient significantly faster than existing one. The proposed FIR channel is implemented on FPGA Spartan-III XC3S50-5PQ208. The proposed serial adder based design is efficient than the conventional adder design in terms of VLSI design environment such as number of slices, LUT and delay.

REFERENCES

[1]. J.A. Howard, S.K. Mitra, and B. Mahbod, "A Novel Single-Multiplier Implementation of IIR and FIR Digital Filters Using Tri-State Logic", IEEE Transactions on Instrumentation and Measurement, Vol. 3, No. 28, 1979, pp. 226-229.

[2]. H.K. Kwan, "A multi-output first-order digital filter structure for VLSI implementation", IEEE Transactions on Circuits and Systems, Vol. 32 ,No. 9, 1985, pp. 973-974.

[3]. A. Huber, E. de Man, E. Schiller, and W. Ulbrich, "FIR Lowpass filter for signal decimation with 15 MHz clock frequency", IEEE International Conference on Acoustics, Speech, and Signal Processing, Vol. 11, 1986, pp. 1533-1536.

[4]. A.G. Dempster, and M.D. Macleod, "Use of minimum-adder multiplier blocks in FIR digital filters" IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing, Vol. 42, No. 9, 1995, pp. 569-577.

[5]. M.A. Soderstrand, L.G. Johnson, H. Arichathiran, M.D. Hoque, and R. Elangovan, "Reducing hardware requirement in FIR filter design" IEEE International Conference on Acoustics, Speech, and Signal Processing, Vol. 6, 2000, pp. 3275-3278.

[6]. K. Nakamura, R. Yamanaka, T. Matsuda, and T. Harada, T, "Recent developments in asymmetric reduction of ketones with biocatalysts", Tetrahedron: Asymmetry, Vol. 14, No. 18, pp. 2659-2681.

[7]. C. Cheng, and K.K. Parhi, "Further complexity reduction of parallel FIR filters" IEEE International Symposium on Circuits and Systems, 2005, pp. 1835-1838.

[8]. R. Conway, "Reducing complexity of fixed-coefficient FIR filters" Electronics Letters, Vol. 42 , No. 20, 2006, pp. 1185-1186.

[9]. C.H. Chang, J. Chen, and A.P. Vinod, "Information theoretic approach to complexity reduction of FIR filter design" IEEE Transactions on Circuits and Systems I, Vol. 55, No. 8, 2008, pp. 2310-2321.