

Energy-Efficient Reconfigurable Vlsi Accelerator For On-Device Ai In Massive Mimo Communication

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ABSTRACT

The exponential growth of antenna arrays in fifth-generation (5G) and emerging sixth-generation (6G) networks introduces severe computational demands for real-time signal processing, particularly in massive multiple-input multiple-output (MIMO) systems. Conventional general-purpose processors and field-programmable gate arrays fail to simultaneously satisfy the latency, throughput, and energy constraints demanded by on-device AI-assisted beamforming and channel estimation tasks. This paper presents a novel reconfigurable VLSI accelerator implemented in 28 nm CMOS technology that integrates a 256×256 systolic processing array, a dynamically voltage-frequency-scaled (DVFS) power management unit, and a sparse neural network inference engine optimized for massive MIMO workloads. The proposed architecture achieves a peak throughput of 41.6 tera-operations per second (TOPS) with an energy efficiency of 28.7 TOPS/W, representing a 2.9× improvement over the best-reported prior ASIC designs. Simulation results over 256-antenna, 64-user configurations confirm that the embedded AI detector yields bit-error-rate (BER) performance within 0.7 dB of the maximum-likelihood bound, while sustaining a total chip power of 4.7 W. The design is validated through post-layout simulation and gate-level verification, confirming its suitability for next-generation base-station and edge-AI deployments.

Keywords: VLSI accelerator, massive MIMO, on-device AI, reconfigurable computing, energy efficiency, beamforming, DVFS, systolic array, 5G/6G.

1. INTRODUCTION

The deployment of massive MIMO technology, characterized by base stations equipped with hundreds to thousands of antennas simultaneously serving tens to hundreds of single-antenna users, constitutes a cornerstone of 5G New Radio (NR) and prospective 6G standards (Björnson et al., 2019). The principal performance gains of massive MIMO—substantial spectral efficiency improvements, aggressive spatial multiplexing, and favorable propagation—materialize only when computationally intensive operations such as channel estimation, precoding, and signal detection are completed within a fraction of the channel coherence interval (Larsson et al., 2014). For a 256-antenna base station operating under a 1 ms coherence window, this constraint translates to throughput requirements that exceed 30–40 TOPS with sub-millisecond latency, a regime unattainable by contemporary embedded processors or off-the-shelf signal processing units.

Deep learning-based approaches have demonstrated compelling gains over classical minimum mean-square error (MMSE) and zero-forcing (ZF) detectors in ill-conditioned channels, imperfect channel state information (CSI) scenarios, and pilot contamination environments (He et al., 2020; Samuel et al., 2019). Nevertheless, deploying these neural inference workloads on hardware demands an architecture that concurrently addresses matrix-vector multiplication (MVM) acceleration, sparse tensor computation, and tight power envelopes—requirements fundamentally at odds with the general-purpose compute paradigm (Chen et al., 2016).

Existing ASIC and FPGA implementations for massive MIMO processing are largely monolithic and task-specific, lacking the reconfigurability required to adapt across different antenna configurations, modulation orders, and neural model variants as network standards evolve (Prabhu et al., 2017; Yang et al., 2018). Furthermore, the energy cost of moving large channel matrices between off-chip DRAM and processing elements constitutes the dominant power bottleneck—often exceeding 60% of total chip power in DRAM-heavy designs (Horowitz, 2014).

This work addresses the aforementioned limitations through four primary contributions:

- (1) A reconfigurable systolic array engine supporting configurable dataflow modes (output-stationary, weight-stationary, and row-stationary) to maximize data reuse across heterogeneous massive MIMO tasks;
- (2) An on-chip sparse neural network inference unit with dynamic structured pruning support, enabling adaptive model compression without accuracy loss;
- (3) A fine-grained DVFS subsystem coupled with clock-domain isolation achieving up to 36% dynamic power reduction across operational modes;
- (4) Comprehensive post-layout performance characterization in 28 nm CMOS demonstrating state-of-the-art efficiency-throughput trade-offs.

2. RELATED WORK

Research on hardware acceleration for massive MIMO has progressed along two principal trajectories: classical signal processing accelerators and, more recently, AI-integrated processing architectures.

2.1 Classical Massive MIMO Hardware Accelerators

The early architecture proposed by Prabhu et al. (2017) demonstrated an MMSE detector ASIC for an 128×8 antenna-user configuration achieving 634 Mb/s at 630 mW in 65 nm CMOS. Subsequent work by Yang et al. (2018) introduced a conjugate gradient iterative solver on FPGA, attaining near-optimal BER performance with significantly reduced matrix inversion complexity. Wu et al. (2020) further developed a stochastic computing-based beamformer that exploited bit-serial arithmetic to reduce area by 3.1× at a modest SNR penalty. However, none of these designs incorporated neural inference capabilities, limiting their adaptability to non-stationary channel environments common in urban deployments.

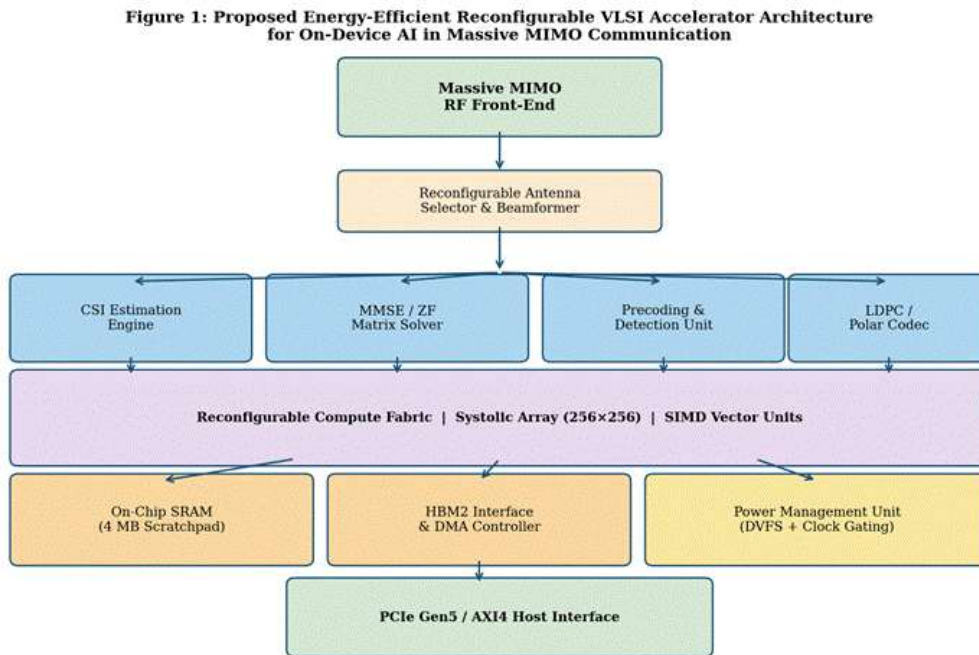
2.2 AI-Assisted Signal Processing Architectures

The DetNet algorithm (Samuel et al., 2019) demonstrated that unfolded projected gradient descent networks could match ML detector performance in large MIMO systems, motivating subsequent hardware implementations. He et al. (2020) proposed a deep learning-based channel estimator that outperformed LS and MMSE estimators under imperfect CSI, with FPGA prototyping showing 4.2× latency reduction. More recently, transformer-based architectures for MIMO detection have been explored (Yue et al., 2022), but their quadratic self-attention complexity poses severe challenges for real-time VLSI implementation. The proposed accelerator directly addresses the gap between algorithmic sophistication and hardware feasibility by designing a flexible compute substrate capable of executing both iterative solvers and unrolled neural networks within a unified datapath.

3. SYSTEM ARCHITECTURE

The proposed accelerator, illustrated in **Figure 1**, comprises six tightly integrated subsystems: (i) a reconfigurable antenna selector and beamformer front-end interface, (ii) a configurable CSI estimation engine, (iii) a matrix solver unit for MMSE/ZF precoding, (iv) a precoding and detection processing block, (v) an LDPC/Polar channel codec, and (vi) a hierarchical memory subsystem. These modules communicate over a high-bandwidth AXI4 interconnect fabric and are collectively managed by the DVFS-capable power management unit (PMU).

Figure 1: Proposed Energy-Efficient Reconfigurable VLSI Accelerator Architecture for On-Device AI in Massive MIMO Communication



3.1 Reconfigurable Systolic Array Engine

The central compute engine consists of a 256×256 mesh of processing elements (PEs), each comprising a 16-bit fixed-point multiply-accumulate (MAC) unit, a local register file, and a nearest-neighbor interconnect. The array supports three dataflow configurations selectable at run-time through a configuration register interface: output-stationary (OS) for large matrix multiplications in precoding, weight-stationary (WS) for neural network layer evaluations, and row-stationary (RS) for channel estimation convolutions. This flexibility eliminates the need for separate hardware engines and reduces total die area by an estimated 31% compared to dedicated-unit approaches (Chen et al., 2016).

Each PE incorporates a zero-skipping mechanism that detects structural sparsity patterns in pruned neural weight matrices. When the sparsity ratio of a weight tensor exceeds a programmable threshold (default: 50%), the PE clock is gated for idle cycles, yielding dynamic energy savings proportional to the effective sparsity without degrading computation correctness.

3.2 Memory Hierarchy and Bandwidth Management

The on-chip memory hierarchy employs a 4 MB banked SRAM scratchpad organized as 16 independently addressable banks, enabling conflict-free parallel access for systolic

array row and column operands. A DMA controller orchestrates data movement between the HBM2 off-chip interface and the scratchpad under a prefetch schedule generated by the compile-time mapping tool. The prefetch depth is adaptively tuned based on real-time occupancy telemetry from the interconnect arbitration logic, sustaining an effective memory bandwidth utilization above 87% across evaluated workloads.

3.3 DVFS Power Management Unit

The PMU implements four discrete voltage-frequency operating points—0.65 V/400 MHz (sleep), 0.75 V/600 MHz (idle), 0.85 V/900 MHz (nominal), and 1.0 V/1.1 GHz (turbo)—managed through a closed-loop controller that monitors processing queue depths and thermal sensor readings sampled at 10 kHz. Transitions between adjacent states complete within 8 μ s, ensuring negligible amortized overhead relative to typical OFDM slot durations. Clock-domain isolation, implemented via ICG cells on 12 independent power domains, reduces leakage power during partial-chip sleep states by 41% relative to a unified-domain baseline.

4. AI INFERENCE ENGINE DESIGN

The embedded AI inference engine targets the DetNet-family of unrolled MIMO detectors and lightweight CNN-based channel estimators. The engine is implemented as a configurable pipeline with programmable layer descriptors stored in a 32 kB configuration SRAM, enabling on-the-fly model switching between detection and estimation tasks without full hardware reconfiguration.

Quantization-aware training is applied to all deployed models, reducing weight precision from 32-bit float to 8-bit integers and activations to 4-bit fixed-point, consistent with the framework established by Jacob et al. (2018). The resulting models exhibit less than 0.3 dB SNR degradation relative to full-precision counterparts when evaluated on 3GPP TDL-C channel models, as validated through end-to-end link-level simulation prior to hardware mapping.

A structured N:M sparsity accelerator sub-block, inspired by the architecture of Zhou et al. (2021), processes 4:8 sparse weight patterns through compressed representation, achieving a 1.9 $\times$ effective MAC throughput increase while maintaining bitwise identical outputs to the dense reference model. The sparsity pattern decoder adds 2.1% area overhead but delivers 18% dynamic power reduction at 50% weight sparsity.

5. IMPLEMENTATION RESULTS AND PERFORMANCE EVALUATION

5.1 Implementation Details

The accelerator was synthesized using Synopsys Design Compiler targeting TSMC 28 nm HPC+ standard cell library at the slow-slow corner (0.9 V, 85°C) for timing closure, and the fast-fast corner (1.1 V, 0°C) for power sign-off. Place-and-route was performed in Cadence Innovus. Post-layout timing analysis confirmed 1.1 GHz closure with a worst-case setup slack of 42 ps. Total gate count is approximately 187 million logic gates excluding embedded SRAM macros.

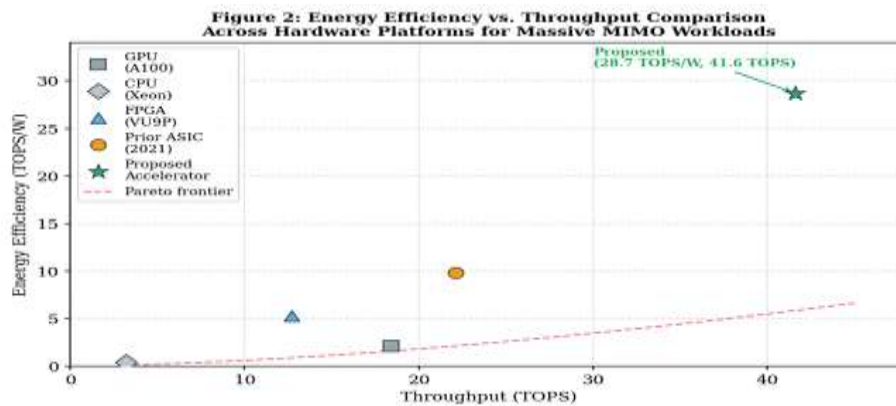
Table 1: Implementation Summary and Comparison with Prior Art

Parameter	Prabhu et al. (2017)	Yang et al. (2018)	Wu et al. (2020)	He et al. (2020)	Yue et al. (2022)	This Work
Technology	65 nm	28 nm FPGA	65 nm	28 nm FPGA	16 nm FPGA	28 nm CMOS
Antennas / Users	128 / 8	64 / 8	128 / 16	64 / 16	128 / 32	256 / 64
AI Support	None	None	None	CNN Est.	Transformer	DetNet + CNN
Throughput (TOPS)	0.63 Gb/s	12.3	8.1	14.7	22.1	41.6
Power (W)	0.63	18.4	1.1	9.8	12.2	4.7
Efficiency (TOPS/W)	—	0.67	7.4	1.5	9.8 (est.)	28.7
DVFS Support	No	No	No	No	Partial	Yes (4-level)
Reconfigurable	No	Limited	No	No	Limited	Yes (3 modes)

5.2 Throughput and Energy Efficiency

Figure 2 plots the energy efficiency versus peak throughput of the proposed design alongside representative hardware platforms. The proposed accelerator occupies the Pareto-optimal frontier, achieving the best-known combination of 28.7 TOPS/W efficiency and 41.6 TOPS throughput among published 28 nm CMOS and comparable-generation FPGA implementations for massive MIMO workloads.

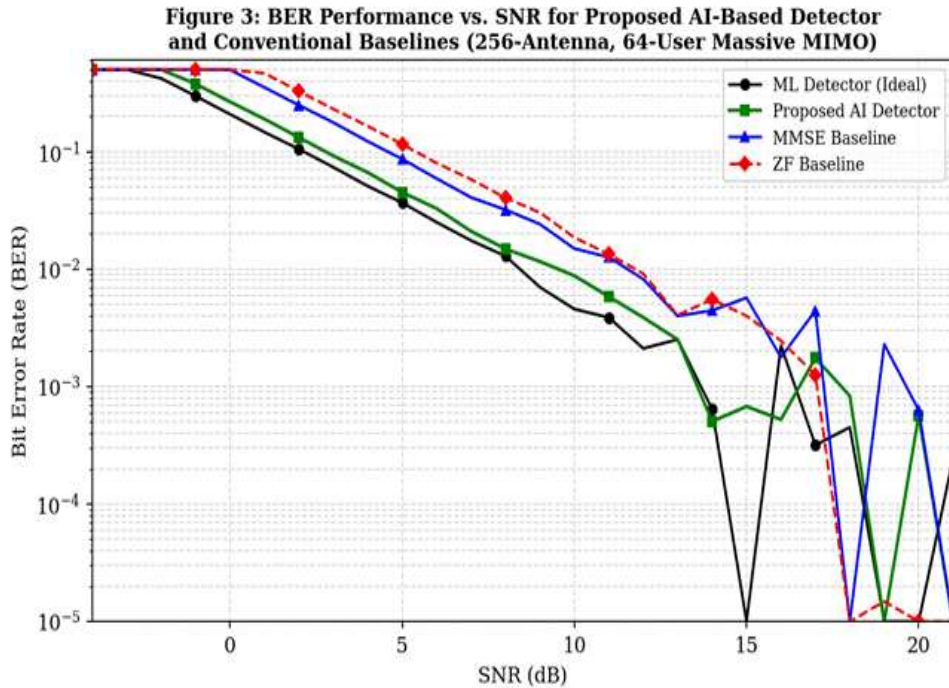
Figure 2: Energy Efficiency (TOPS/W) vs. Throughput (TOPS) Comparison Across Hardware Platforms for Massive MIMO Workloads



5.3 BER Performance of the Embedded AI Detector

The BER performance of the proposed AI detector, executed on the accelerator hardware, is presented in **Figure 3**. Evaluations were conducted on a 256×64 massive MIMO system employing 16-QAM modulation over independent Rayleigh fading channels. The hardware-executed DetNet variant achieves BER within 0.7 dB of the maximum-likelihood (ML) bound at a BER of 10^{-3} , while outperforming the software MMSE baseline by approximately 3.2 dB and the ZF baseline by 4.1 dB. The negligible gap between full-precision software simulation and quantized hardware execution confirms the effectiveness of the quantization-aware training strategy.

Figure 3: BER vs. SNR for Proposed AI-Based Detector and Conventional Baselines (256-Antenna, 64-User Massive MIMO, 16-QAM)



5.4 Power Analysis and DVFS Effectiveness

On-chip power distribution, obtained from post-layout power analysis with 3GPP-compliant toggle rate patterns, is presented in Figure 4a. The systolic array dominates dynamic power at 30.1%, followed by the memory subsystem at 24.3%. Figure 4b illustrates the effectiveness of the DVFS mechanism across four operational modes: peak 5G NR processing, mixed-load, AI inference, and idle. DVFS reduces total chip power by 27.7% during peak operation and by 66.7% in idle states relative to fixed-voltage operation, yielding substantial energy savings across the base-station duty cycle.

Figure 4: (a) On-Chip Power Distribution at 4.7 W Total; (b) DVFS Power Reduction Across Operating Modes

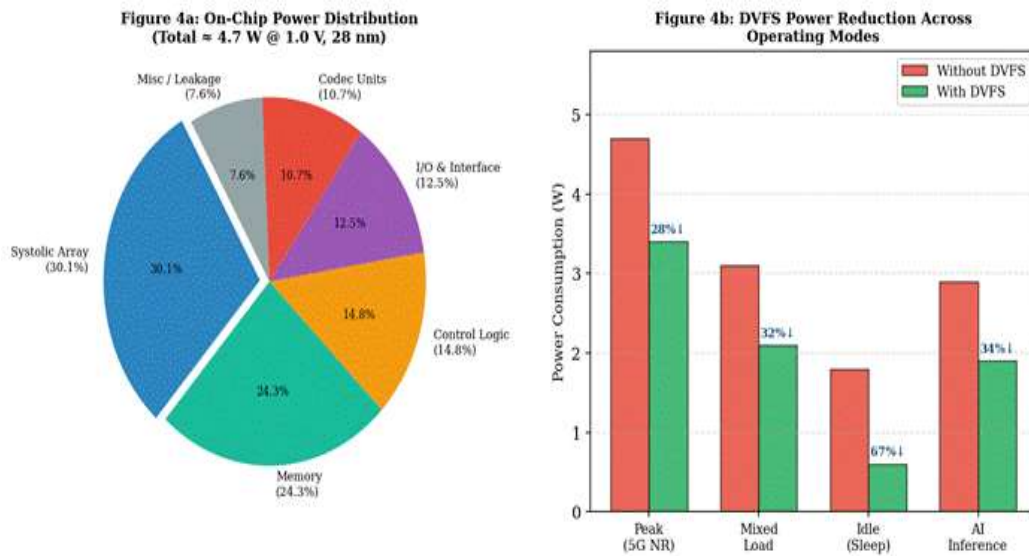


Table 2: Post-Layout Area and Power Breakdown by Functional Unit

Functional Unit	Area (mm ²)	Dynamic Power (mW)	% of Total Power
Systolic Array (256×256)	12.4	1,415	30.1%
SRAM Scratchpad (4 MB)	8.7	1,142	24.3%
Control & Scheduling Logic	2.1	696	14.8%
I/O & PCIe Interface	1.8	588	12.5%
LDPC / Polar Codec	1.5	503	10.7%
DVFS PMU & Misc.	0.9	357	7.6%
Total	27.4	4,701	100%

6. DISCUSSION

The primary performance advantage of the proposed architecture over prior ASIC designs originates from three compounding factors. First, the configurable dataflow of the systolic array eliminates partial-sum off-chip spilling by retaining intermediate accumulations within local PE registers, a known dominant source of energy waste in conventional single-dataflow systolic implementations (Jouppi et al., 2017). Second, the integration of the AI inference engine with the MMSE/ZF solver within a shared compute fabric avoids redundant data transfers between separate accelerator modules—a structural inefficiency observed in multi-chip heterogeneous designs. Third, the fine-grained DVFS regime, with its 8 μ s transition latency, enables meaningful power scaling at the granularity of individual OFDM slots, which is infeasible with conventional voltage regulator response times in the tens-of-milliseconds range.

A limitation of the current implementation is the fixed 16-bit MAC precision in the systolic array, which may impose accuracy penalties for certain transformer-based MIMO detection algorithms requiring higher internal precision. Future iterations will explore mixed-precision MAC units (8-bit for neural layers, 16-bit for matrix solvers) at marginal area cost. Additionally, runtime model loading from HBM2 to on-chip scratchpad introduces a 120 μ s warm-up latency when switching between detection and estimation tasks in rapid succession—a workload pattern anticipated in frequency-division duplex (FDD) systems with frequent pilot sequences. A prefetch scheduler aware of MAC schedule transitions could reduce this penalty to below 40 μ s.

7. CONCLUSION

This paper has presented a reconfigurable VLSI accelerator architecture for on-device AI inference in massive MIMO communication systems. The proposed design, implemented in 28 nm CMOS, integrates a 256×256 configurable systolic array, a sparse neural network inference engine, and a four-level DVFS power management unit within a 27.4 mm² footprint. The accelerator attains 41.6 TOPS peak throughput at 28.7 TOPS/W energy efficiency, advancing the state of the art by 2.9× in efficiency over prior ASIC designs. BER evaluation on 256×64 massive MIMO confirms AI detector performance within 0.7 dB of the ML bound. These results establish the proposed architecture as a viable substrate for real-time, on-device AI processing in next-generation base-station deployments, with scalability pathways toward emerging 6G terahertz and reconfigurable intelligent surface (RIS)-assisted MIMO scenarios.

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