

## ***Design And Implementation Of Innovative Methodologies And Architectures For Digital Signal Processing On Fpgas***

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### ***Abstract***

The recent advances in real-time applications in communication, biomedical systems, radar, and intelligent computing applications have boosted the need of high-performance and energy-efficient digital signal processing (DSP) systems. FPGAs have become a powerful solution to this problem because they are able to process data in parallel at a time and can be reconfigured, as well as they have guaranteed timing. The current paper represents a systematic review of optimization strategies and architectural development of FPGA-based DSP implementations that were published after 2020. With the PRISMA model, the relevant selection of journal articles was identified, screened, and further analyzed to provide a clear and systematic review procedure. A list of 62 articles was chosen out of an initial list of 1970 articles retrieved and searched through the SCOPUS database. The analysis of the important design techniques identifies high-level synthesis technique, hardware software co-design technique, pipelining, parallel architecture techniques, and precision optimization techniques such as quantization-aware design technique. The results present major advances in performance, resource consumption, power efficiency and numerical accuracy at a variety of applications, such as artificial intelligence; secure communication and biomedical signal processing. The paper also addresses the issues that exist and also outlines the future research avenues in the area of scalable and efficient FPGA-based DSP systems.

**Keywords:** Digital Signal Processing, FPGA, Optimization Techniques, Hardware-Software Co-design, PRISMA Systematic Review.

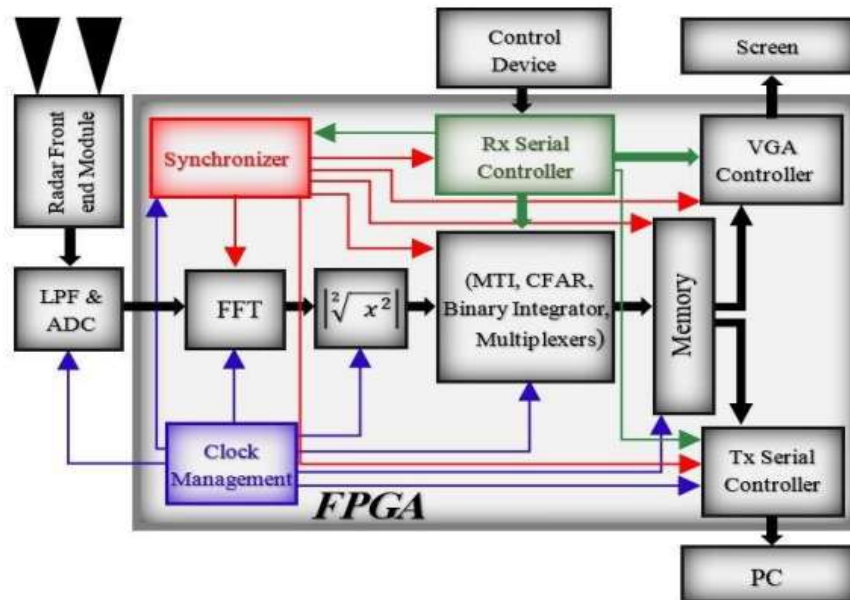
### ***1. Introduction***

The fast development of digital communication, multimedia, biomedical instrumentation, radar and embedded intelligence systems has greatly augmented the need of high-speed and low-latency and low-energy consumption signal processing platforms [1]. Digital Signal Processing (DSP) is a crucial factor in facilitating these new applications since it works in real-time, e.g., filtering, modulating, compressing, feature detection, and spectral analysis [2]. Conventional processor-based solutions are often not able to provide the performance and timing requirements when system complexity and data rates keep increasing [3]. Here, Field Programmable Gate Arrays (FPGAs) have become an influential and versatile hardware platform to execute high-performance DSP systems [4].

The FPGAs have a massive parallelism, re-configurability and deterministic timing that render it very appropriate in DSPs with computation-intensive responsibilities [5]. FPGAs also enable the designer to experiment with fine-grained parallel architectures, pipeline structures and custom data paths that are highly suitable in particular signal processing algorithms as opposed to general-purpose processors [6]. This degree of software integration at the hardware level has tremendously increased throughput and greatly reduced latency, and power efficiency has not been compromised [7-9]. Once more, the contemporary FPGAs have dedicated DSP slices; block RAMs, high-speed transceivers and hardware multipliers which further increase the ability of the FPGA to

support very complex real-time DSP applications [10]. The developed digital signal processing block diagram with the use of FPGA is presented in Figure 1.

**Figure 1: Developed Digital Signal Processing block diagram using FPGA [11].**



Designing efficient DSP systems on FPGAs is a challenging task due to constraints such as limited hardware resources, power consumption, timing closure, and scalability [12]. Traditional design methodologies based on low-level hardware description languages often require long development times and necessitate deep expertise in digital hardware design [13]. Optimizing DSP algorithms for FPGA architectures requires careful consideration of parallelism, pipelining, fixed-point arithmetic, memory access patterns, and clock domain management. These challenges highlight the need for innovative methodologies and architectural strategies that can simplify development while maximizing performance and resource efficiency [14].

The design and development of novel methodologies and architectures for DSP on FPGAs aim at filling the divide that exists between algorithm design and implementation on hardware systems [15]. New design methodologies such as High-Level Synthesis (HLS), model-based design, and hardware-software co-design have significantly changed the design process by enabling designers to design DSP algorithms using high-level languages such as C, C++, MATLAB, or Python. This is followed by the automatic generation of optimized hardware descriptions [16].

Along with new design approaches, architectural innovations are also significant in fulfilling the ideal DSP performance at FPGAs [17]. Pipelined architectures, parallel processing engines, systolic arrays and reconfigurable processing elements allow easiness in mapping DSP algorithms to hardware. Loop unrolling, dataflow optimization, and memory partition techniques are some of the techniques that are useful in exploiting the parallelism which exists in signal processing algorithms [18]. Moreover, reconfigurable and adaptive architectures enable the FPGA-based DSP systems to dynamically change to different signal conditions, data rates and application needs, enabling them to be used in next-generation intelligent systems [19].

The other consideration in the FPGA-based DSP design is the heterogeneous computing resources. Contemporary FPGAs are programmable logic controllers, which integrate embedded processors, hardware accelerators, and high-speed interfaces onto a single chip [20]. This facilitates the deployment of hybrid designs in which processes that require little complexity and control are executed on processors and those that require significant amount of computation are offloaded to hardware accelerators [21]. These heterogeneous architectures enhance the overall performance of a system and are more energy efficient in addition to offering software programmability and flexibility at system level.

With the growing popularity of artificial intelligence [22], 5G/6G communication, Internet of Things (IoT) [23], and autonomous systems [24], the application of FPGA-based DSP is also becoming more popular [25]. These applications involve processing of large volumes of data in realtime with a high level of speed and reliability requirement. These new challenges can be handled by new designs of FPGA and smart design techniques that are now able to develop scalable, reconfigurable, and high-throughput DSP platforms.

In this case, optimization systems and accuracy study of DSP models in FPGAs are highly significant in the field of research and development. FPGA-based DSP systems can be designed with superior hardware architectures through advanced design techniques to perform better, have flexibility and be energy efficient. This not only enhances the reality of using DSP solutions in the real world applications but also provides avenues of future smart and dynamic signal processing platform.

### 1.1 Field-Programmable Gate Array (FPGA)

FPGAs are reconfigurable semiconductor chips, which enable designers to design custom digital hardware even after the manufacturing of the chips [26]. FPGAs differ from ASICs because, on one hand, ASICs are fixed chips once manufactured, and on the other hand, FPGAs can be programmed and reprogrammed to perform numerous tasks [27]. FPGAs are extensively utilized in various domains like digital signal processing, telecommunication, embedded systems, aerospace, automotive electronics, and artificial intelligence acceleration due to their re-configurability and numerous other advantages [28].

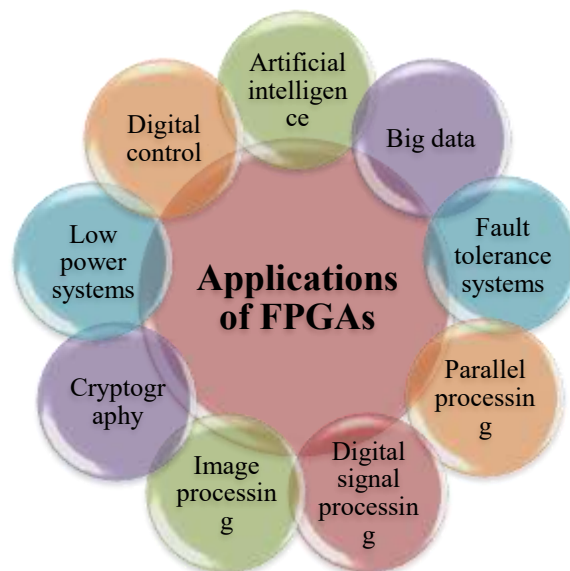
**Table 1: ASIC vs FPGA Comparison**

| <b>FPGA</b>                                            | <b>ASIC</b>                                            |
|--------------------------------------------------------|--------------------------------------------------------|
| Reconfigurable circuitry after manufacturing           | Fixed circuitry for product's lifespan                 |
| Suitable for digital designs only                      | Analog/mixed-signal circuitry can be fully implemented |
| Can be purchased as off-the-shelf products             | Can only be designed as custom, private-label devices  |
| Lower performance efficiency, higher power consumption | Low power consumption, high performance efficiency     |
| No non-recurring engineering (NRE) costs               | NRE costs are part of the design process               |
| Difficult to attain high-frequency rates               | Operate at higher frequency rates                      |
| Faster time-to-market, higher per-unit costs           | Long time-to-market, lower per-unit costs              |
| Typically larger than ASICs                            | Can be much smaller than FPGA                          |

|                                        |                                                                    |
|----------------------------------------|--------------------------------------------------------------------|
|                                        | devices                                                            |
| Easier prototyping and validation      | Prototypes must be accurately validated to avoid design iterations |
| Lower barrier to entry for competitors | Higher barrier to entry for competitors                            |

An FPGA is made up of a matrix of configurable logic blocks (CLBs), interconnects that can be programmed, and input/output (I/O) blocks [29]. The logic blocks usually have look-up tables (LUTs), flip-flops, and multiplexers that can be set up to realize both combinational and sequential logic [30]. The programmable routing network permits these blocks to be connected in almost any configuration desired enabling the complex digital circuits' creation [31]. Contemporary FPGAs also include specific hardware resources like block RAM, digital signal processing slices, phase-locked loops, and high-speed transceivers to aid high-performance applications. Figure 2 displays the applications of FPGAs [32,33].

**Figure 2: Applications of FPGAs [34]**



The ability to take advantage of great parallelism is one of the main benefits of FPGAs. Microprocessors execute instructions in a sequential order; however, FPGAs have the capability to carry out multiple processes at the same time [35]. This quality makes them perfect for use in tasks that require much computation power such as real-time signal processing, video processing cryptography as well as machine learning inference [36]. Moreover, FPGAs provide low latency and deterministic timing which play an essential role in systems that require real-time performance and those that are critical for safety.

In summary, FPGAs offer a strong and flexible platform for creating personalized digital systems with high performance and adaptability [37]. Their ability to be reprogrammed, process things at the same time, and have many built-in resources make them a preferred choice in both research and industrial uses, helping connect general-use processors with hardware accelerators that cannot change [38].

## **2. Research Methodology**

In the paper, the review of optimization models and accuracy analysis methods of DSP models on FPGA platforms between 2020 and 2025 is provided. It talks about the recent developments in custom hardware-software co-design systems that enhance computational performance, resource usage, power and numerical precision of DSP algorithms on reconfigurable architectures. Different optimization methods used to improve the real-time signal processing performance are reviewed as fixed-point precision tuning, quantization-aware design, parallel processing, and pipeline architectures. The PRISMA approach is used to conduct the review, which is a systematic and clear study selection and evaluation process consisting of three important steps, namely, planning, search, and analysis. This methodology will allow classifying and comparing the available techniques of the optimization of FPGA-based DSPs and finding open gaps in terms of scalability, precision trade-offs, and hardware limitations. The results give a prospective research the basis by pointing out gaps in research and inform how research can be effective and precise in implementing the DSP code on the FPGA platform as well as its derivatives.

### **2.1 Planning Stages**

The applications of high-performance DSPs need hybrid hardware-software architectures to create special FPGA-based processing models with high computational accuracy and low latency, power, and resource overhead. FPGA environments are dynamic and of heterogeneous nature, which encompasses different signal modalities, different sampling rates, real time processing limitations and time varying algorithmic demands. These properties present strong difficulties with the creation of effective and accuracy-conscious DSP systems. To tackle these issues, scholars use superior optimization methods, such as heuristic and meta-heuristic algorithms, to enhance model flexibility, numerical soundness, and the general performance of the systems. These techniques allow multimodal signal data to be effectively processed by the DSP models, and appropriate and dependable outputs can be produced by them within the constraints of real-life operations.

This study provides an extensive literature review of optimization frameworks and accuracy estimation methods for FPGA-based DSP implementations published between 2020 and 2025. It captures the changing architectural trends and optimization approaches over the years. The research is organized around these questions:

- (i) What emerging optimization frameworks between 2020 and 2025 are shaping the development of high-performance DSP systems on FPGA platforms?
- (ii) Which hybrid hardware-software models demonstrate the highest accuracy, efficiency, and resource utilization for real-time DSP applications?
- (iii) What major technical challenges arise in precision tuning, quantization, and hardware resource management for FPGA-based DSP implementations?
- (iv) How can emerging reconfigurable computing techniques and adaptive precision control enhance the reliability, scalability, and performance of FPGA-based DSP systems?

The literature review retrieves its corpus primarily from the SCOPUS database using keyword-based queries such as "Digital Signal Processing," "Fpga," "Field Programmable Gate arrays (fpga)," and "Signal Processing." The study have been chosen from diverse sources such as digital signal processing, embedded systems, reconfigurable computing, and hardware engineering, with specific focus on designing, optimizing, and implementing DSP models on FPGA. Taken together, this review article describes

present methods used for increasing accuracy in signal processing in real time, optimizing numerical accuracy, minimizing latency time.

## 2.2 Review Stages

The review process is guided with laid down inclusion and exclusion criterion that is of paramount help in the selection of quality research articles. The inclusion and exclusion criteria for the literature search are as follows:

- i. Research publications published from 2020 to 2025 are eligible for inclusion in the review for the SCOPUS database,
- ii. Excluding the document other than article,
- iii. Only journal articles are included; conference papers, books, and other document types are excluded.
- iv. Articles that are not in the English language are excluded to maintain consistency and relevance.

Table 2 presents the inclusion and exclusion criteria applied for selecting relevant research articles.

**Table 2: The criteria for determining what is included and excluded**

| <b>Criterion</b>     | <b>Inclusion</b>                                                                          | <b>Exclusion</b>                                     |
|----------------------|-------------------------------------------------------------------------------------------|------------------------------------------------------|
| <b>Keywords</b>      | Digital Signal Processing, Fpga, Field Programmable Gate arrays (fpga), Signal Processing | Records excluded in which variables have no relation |
| <b>Document Type</b> | Article                                                                                   | Conference paper, Review and Erratum                 |
| <b>Source Type</b>   | Journals                                                                                  | Book series, book, and chapter in book.              |
| <b>Language</b>      | English                                                                                   | Other than English                                   |
| <b>Timeframe</b>     | Concerning 2020-2025                                                                      | <2020                                                |

**Figure 3: PRISMA Model for literature analysis**

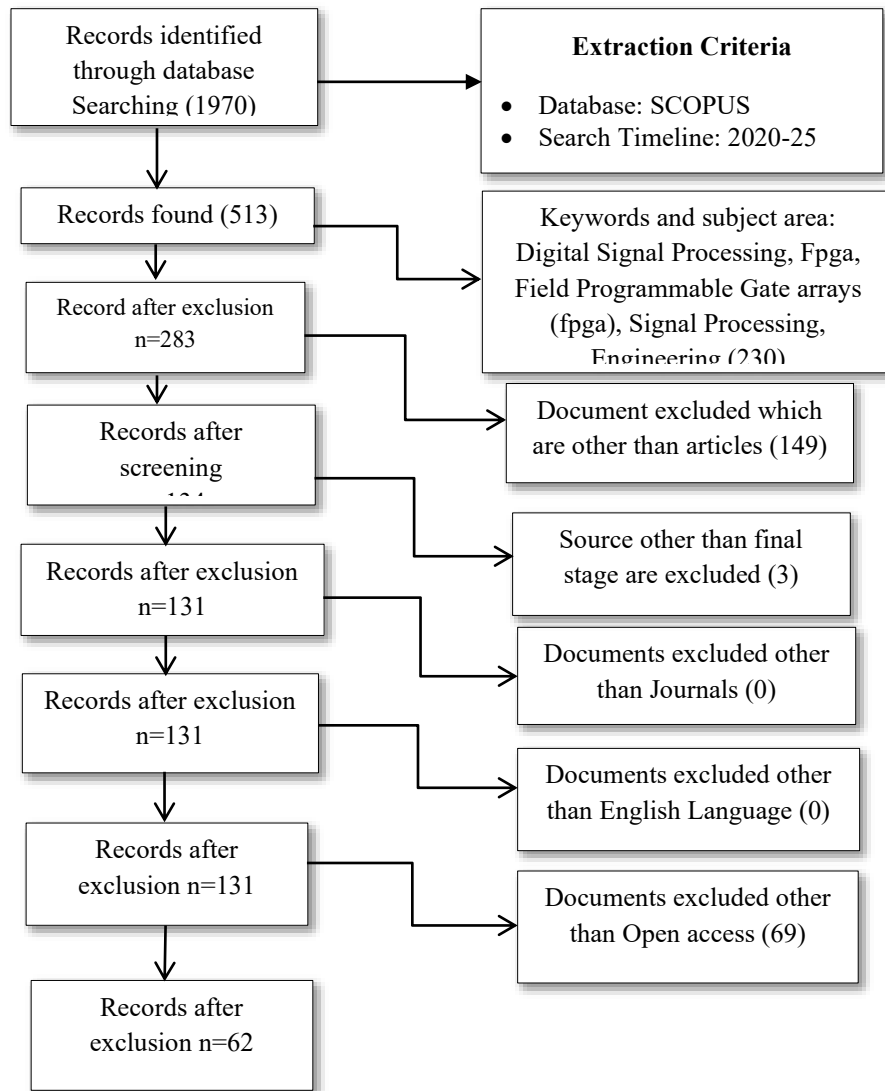
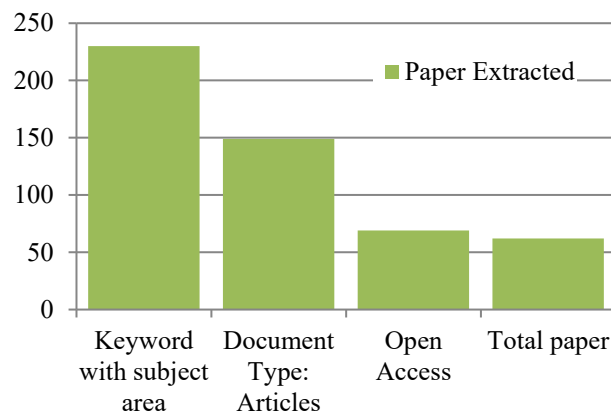


**Figure 4: Graphical representation of PRISMA model**



Systematic filtering was carried out according to the defined retrieval criteria, as illustrated in Figure 3 using the PRISMA model. Furthermore, Figure 4 presents the graphical representation of the PRISMA model based on the extracted studies. Comprehensive search was first conducted in SCOPUS using the keywords “Digital Signal Processing,” “Fpga,” “Field Programmable Gate arrays (fpga),” and “Signal Processing” as topics in Engineering during the timeframe of 2020 to February 22, 2025, yielded 513 records in total. In the initial filtering, 149 non-article documents were deleted and the count reached 134. Further filtering also deleted three sources other than journal sources, and the count dipped to 131. Further, zero documents whose language was different from English were deleted and there remained 131 records. The last filtering stage eliminated 69 non-open access documents, leaving a total of 51 papers for final analysis. The chosen documents align with the research objectives and meet all pre-specified inclusion criteria for further evaluation.

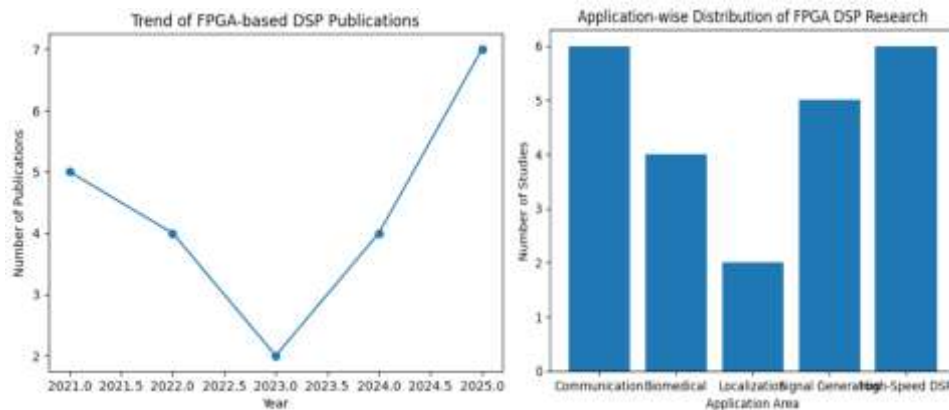
### **3. Design and Implementation of Innovative Methodologies and Architectures for Digital Signal Processing on FPGAs**

Their intrinsic parallel nature, flexibility through re-configurability, as well as real-time applicability has seen FPGAs become a widespread hardware platform to design high-performance DSP systems. Chiou et al. (2025) [37] illustrated the FPGA-based localization and tracking hardware models of real-time location-based services that included triangulation and path-loss models as well as barometric pressure sensors. Their pipelined hardware design was efficient in facilitating the floating point operations besides showing localization accuracy as compared to software based implementations. A major area of DSP uses of FPGAs is in waveform generation and digital modulation. Having a large number of LUTs and block RAM, Nassim et al. (2025) [38] described a direct digital synthesis (DDS) sine wave generator on a Spartan-6 FPGA on-the-fly frequency and phase-controlled suitable to modulation schemes like BPSK. Another limitation of DDS was covered by Xing et al. (2024) [39], who suggested building a recursive trigonometry-based architecture that removes the memory of look-up tables and allows much less power and memory usage without decreasing the quality of the waveforms.

Software-defined radio (SDR) and communication systems have also been researching advanced ways of modulating them. Tchendjeu et al. (2025) [40] created a numerical solver-based QPSK modulator that uses an FPGA, about which the negative impedance converter is implemented, without memories and embedded multipliers. The design used more logic resources, however, it allowed deterministic behavior and caused less dependency on storage. Capligns et al. (2025) [41] suggested a chaotic digital system of communication based on Cyclone-V FPGA, which had resistance to noise and was capable of providing secure communications with the aid of frequency-modulated chaos

shift keying. Filtering and sample-rate conversion are still fundamental DSP issues that are solved with the FPGA architectures. A study by Talal et al. (2025) [42] utilized the polyphase-based architecture to implement decimators, interpolators and sample-rate converters on an Artix-7 FPGA and demonstrated that polyphase architectures consumed much less hardware than their different structural realizations. Gadawe et al. (2024) [43] investigated the IIR filter implementation in FPGA using ECG signal processing and came to the conclusion that cascaded and retimed structures help to attain limitations of efficient real-time applications. Xu et al. [44] further improved the application of the filters by developing a hardware-efficient implementation of the fractional Kalman filters with the Grunwald-Letnikov approximation to save a lot of resources consumed by the implementation of the Kalman filters used on FPGA platforms.

**Figure 5: Trend of FPGA-based DSP Publications (2021–2025) and Application-wise Distribution of FPGA DSP Research**



FPGA accelerator has been used in bio-inspired and biomedical applications of DSP. A digital circuit of a modified artificial cochlea on trigonometric approximations and terms of base-2 with CORDIC algorithms was proposed by Chen et al. (2025) [45]. The design has done away with multipliers and has been able to operate at higher frequencies with their behavior comparable to the cochlear behavior. Sajjad et al. (2021) [46] concentrated on sensor signal conditioning by setting out to create a programmable FPGA-based architecture of the barometric pressure sensor being used to create a high degree of accuracy regardless of the variations in the environment. DSP systems with high-speed and ultra-wideband pose exceptionally rigid demands in terms of timing and throughput. Canese et al. (2024) [47] introduced a parallel FPGA design of ultra-wideband equalization that was able to perform signal processing at the frequency of GHzs wholly within the typical FPGA clock bands. Lee et al. (2022) [48] onboard reduced SAR Data was further discussed by using an FPGA implementable modified discrete Fourier transform filter bank, that delivered a better data reduction compared to the established dechirp-on-receive methodologies. Such works show the presence of FPGA in signal processing applications with high bandwidth requirements.

Another FPGA important application area is precision timing and measurement systems. Portaluppi et al. (2022) [49] designed a multi-channel time-to-digital converter with a resolution of picoseconds on delay lines in the form of carry chains. Garzetti et al. (2021) [50] also investigated tapped delay-line architectures at the different nodes of the FPGA technology, reaching a precision of femtoseconds. To confirm the appropriateness of FPGA in ultra-high-resolution time measurements, Charlot et al. (2021) [51] presented a

waveform capture device that has the capability to record signals with kilosecond time scales at picosecond time scales by FPGA carry chains. More attention has been focused on energy-efficient and lower-precision DSP implementations. Corda et al. (2022) [52] showed that energy consumption in radio astronomy images with reduced-precision floating-point arithmetic on FPGAs can reduce energy consumption by a significant margin without reducing the image quality. Applying the trade-off of complexity between systems and performance, Donadello et al. (2023) [53] demonstrated that some optical signal processing applications can be dealt with by embedded microcontrollers in place of an intricate FPGA system.

**Table 3: Literature of Review (LOR) DSP on FPGAs**

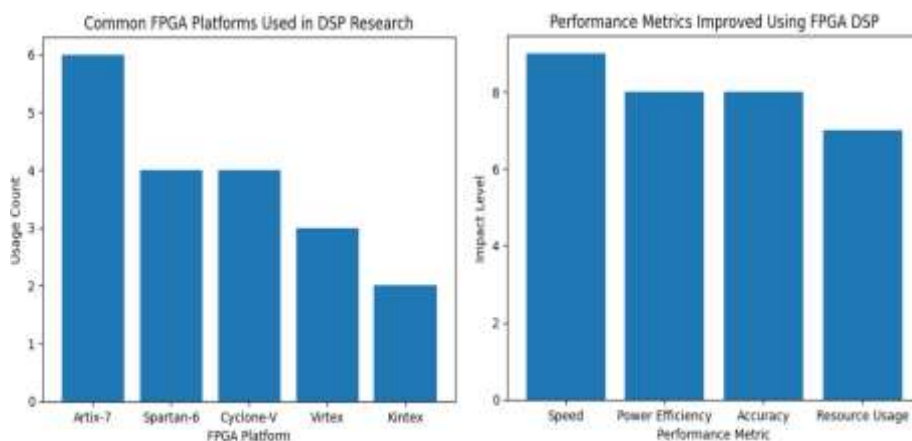
| <b>Author (Year)</b>    | <b>Application Area</b>    | <b>FPGA / Platform Used</b> | <b>Methodology / Architecture</b>               | <b>Key Contribution</b>                                      | <b>Main Outcome</b>                                                |
|-------------------------|----------------------------|-----------------------------|-------------------------------------------------|--------------------------------------------------------------|--------------------------------------------------------------------|
| Chiou et al. (2025)     | Localization & Tracking    | FPGA with BP sensors        | Pipelined triangulation and tracking algorithms | Integrated horizontal and vertical localization using FPGA   | Achieved real-time processing with accuracy comparable to software |
| Nassim et al. (2025)    | Signal Generation          | Spartan-6 FPGA              | DDS using LUTs, BRAM, and DAC                   | Flexible frequency and phase-controlled sine wave generation | High-quality waveform generation with low power                    |
| Porreca et al. (2025)   | Wearable Systems           | FPGA + MCU                  | Mixed hardware–software framework               | Efficient far-edge computing for wearables                   | Improved speed and reduced power consumption                       |
| Tchendjeu et al. (2025) | Digital Communication      | DE2-115 FPGA                | NIC-based digital oscillator for QPSK           | Memory-less QPSK modulation                                  | Suitable for low-storage, secure communication                     |
| Talal et al. (2025)     | Sample Rate Conversion     | Artix-7 FPGA                | FIR-based decimator, interpolator, SRC          | Comparison of direct, efficient, polyphase structures        | Polyphase design reduced hardware usage                            |
| Chen et al. (2025)      | Auditory Signal Processing | Virtex-II FPGA              | Artificial cochlea model using CORDIC           | Multiplier-free cochlea modeling                             | Higher speed and lower hardware                                    |

|                          |                          |                         |                                      |                                           |                                               |
|--------------------------|--------------------------|-------------------------|--------------------------------------|-------------------------------------------|-----------------------------------------------|
|                          |                          |                         |                                      |                                           | cost                                          |
| Capligns et al. (2025)   | Secure Communication     | Cyclone V FPGA          | FM-based chaotic modulation          | FPGA-based chaotic communication system   | Improved noise robustness and security        |
| Węgrzyn et al. (2025)    | Mathematical DSP         | FPGA-based system       | Floating-point SQRT using CORDIC     | Fast and accurate square-root computation | Suitable for ML, vision, and DSP applications |
| Xing et al. (2024)       | Frequency Synthesis      | Lattice FPGA            | Recursive Trigonometry DDFS          | LUT-free waveform generation              | Reduced power and memory usage                |
| Gadawe et al. (2024)     | Biomedical DSP           | Artix-7 FPGA            | FPGA-based IIR filters for ECG       | Evaluation of filter structures           | Real-time ECG processing achieved             |
| Canese et al. (2024)     | Ultra-Wideband DSP       | Kintex Ultrascalar FPGA | Parallel equalizer with Block LMS    | GHz-level signal processing               | Overcame FPGA clock limitations               |
| Lee et al. (2022)        | Spaceborne SAR           | Space-grade FPGA        | MDFT-based data reduction            | Reduced onboard data volume               | Better data reduction than DoR                |
| Xu et al. (2022)         | Control Systems          | FPGA                    | Fractional Kalman Filter             | Resource-efficient FKF implementation     | Faster real-time filtering                    |
| Portaluppi et al. (2022) | Time Measurement         | Artix-7 FPGA            | TDC using carry-chain delay lines    | Picosecond-level resolution               | High accuracy and linearity                   |
| Corde et al. (2022)      | Radio Astronomy          | Xilinx Alveo U50        | Reduced-precision FPGA accelerator   | Custom floating-point design              | Improved energy efficiency                    |
| Sajjad et al. (2021)     | Sensor Signal Processing | Spartan-6 FPGA          | Polynomial compensation architecture | Programmable sensor calibration           | High accuracy and flexibility                 |
| Garzetti et al. (2021)   | Timing Circuits          | Xilinx 7-Series FPGA    | Asynchronous TDL-based TDC           | High-resolution time measurement          | Sub-picosecond precision achieved             |

|                         |                           |                        |                               | ent                               |                                  |
|-------------------------|---------------------------|------------------------|-------------------------------|-----------------------------------|----------------------------------|
| Donadello et al. (2023) | Optical Signal Processing | Dual-core MCU          | Embedded DSP architecture     | FPGA alternative for optical DSP  | Lower cost and power consumption |
| Charlot et al. (2021)   | High-Speed Measurement    | Cyclone V FPGA         | Waveform Capture Device       | ps-scale signal capture           | Accurate waveform reconstruction |
| Huang et al. (2021)     | Optical Communication     | FPGA-based SPAD system | Real-time photon-counting DSP | Reliable underwater communication | Very low BER achieved            |

Huang et al. (2021) [54] described a real-time underwater photon-counting comms system implemented on FPGA that achieves low bit error rates with efficient synchronization and channel coding. Sharma et al. (2021) [55] proposed an architecture based on FPGA quadrature down-conversion for ultra-wideband spectrum analysis, which simplifies RF front-end complexity yet offers performance in image rejection. Finally, architectural frameworks and algorithmic optimizations keep enhancing the usability of FPGAs. Porreca et al., 2025 [56], described a mixed FPGA/MCU development framework for wearable systems; it was shown to improve execution speed and power efficiency for far-edge computing. Węgrzyn et al., [57] presented an optimized floating-point square root CORDIC algorithm implemented in 2025 that has low complexity but high speed applicable to DSP as well as machine learning accelerators.

**Figure 6: Common FPGA Platforms Used in DSP Research and Performance Metrics Improved Using FPGA DSP**



#### 4. FPGA-Based Architectures for Artificial Intelligence and Neural Networks

Researchers now conduct their studies about artificial intelligence and neural network systems through FPGA-based architecture design because they need energy-saving solutions which enable simultaneous processing and instant computational results. Bosso et al. (2025) [58] show how activation function optimization matters by introducing a polynomial-based sigmoid approximation which requires minimal FPGA

resources while delivering high accuracy results. In their research Hingu et al. (2024) [59] developed a hardware implementation for the tanh function that uses continued fraction and polynomial methods through which they achieved lower power consumption and reduced logic requirements while maintaining high numerical precision. In their research study Moroz et al. (2023) [60] present piecewise linear methods which provide low-complexity exponential function approximations that work effectively in neural network accelerator systems which require minimal processing power.

Kokkinis et al. (2025) [61] present design automation and rapid prototyping solutions through their creation of a quick resource estimator which operates with the hls4ml workflow to assess FPGA-based multilayer perceptron systems. Their approach enables quick feasibility analysis for TinyML applications. The studies by Ahmad et al. (2021) [62] and Paz et al. (2023) [63] show how designers can achieve power and area reductions through the use of approximate adders and DSP-based multipliers which still provide acceptable accuracy.

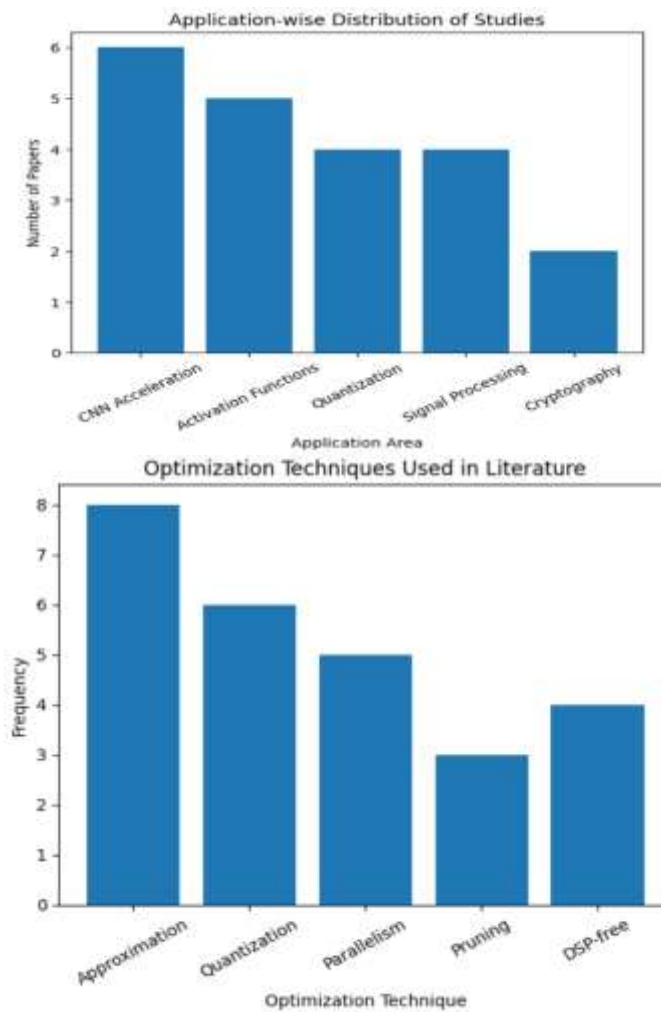
**Table 4: LOR based on FPGA-Based Architectures for AI and Neural Networks**

| <b>Authors (Year)</b>      | <b>Focus Area</b>           | <b>Methodology / Approach</b>                        | <b>Key Contribution</b>                                            |
|----------------------------|-----------------------------|------------------------------------------------------|--------------------------------------------------------------------|
| Bosso et al. (2025)        | Activation Function         | Polynomial approximation of sigmoid                  | Achieved low approximation error with very low FPGA resource usage |
| Kokkinis et al. (2025)     | TinyML / Design Automation  | Resource estimation for MLPs using hls4ml            | Fast and accurate prediction of LUT, FF, and DSP usage             |
| Hingu et al. (2024)        | Activation Function         | Continued fraction and polynomial tanh approximation | Reduced power and resource consumption with high accuracy          |
| Jiang et al. (2024)        | Neural Network Architecture | Adaptive activation function with SSCNN              | Comparable DNN accuracy using fewer FPGA resources                 |
| Campos et al. (2024)       | Image Processing            | Custom floating-point spatial filters                | Real-time 1080p video processing on low-cost FPGA                  |
| Fuketa et al. (2024)       | CNN Acceleration            | Residual lookup-table dot product (RLDA)             | Multiplier-free CNN inference with minimal accuracy loss           |
| Sakamoto et al. (2024)     | Cryptography                | DSP-optimized pairing processor                      | Achieved high throughput for server-side FPGA applications         |
| Tariq et al. (2024)        | Signal Processing           | Parallel particle filter accelerator                 | Improved speed and reduced area for real-time tracking             |
| Senthilkumar et al. (2023) | Biomedical AI               | ICA-based RNN on FPGA                                | Low-power real-time ECG signal analysis                            |
| Pistellato et al. (2023)   | Quantized Neural Networks   | Trainable requantization layers                      | Near-floating-point accuracy with ultra-low precision              |

|                       |                          |                                            |                                                          |
|-----------------------|--------------------------|--------------------------------------------|----------------------------------------------------------|
| Yang et al. (2023)    | CNN Framework            | Unified FPGA CNN architecture              | Improved DSP utilization and inference speed             |
| Hassan et al. (2023)  | Neural Signal Processing | Approximate computing on FPGA              | Enhanced speed and reduced area with acceptable accuracy |
| Nevarez et al. (2023) | Quantization             | Hybrid-Float6 MAC architecture             | High power efficiency using quantization-aware training  |
| Lehnert et al. (2023) | ANN Optimization         | Weight matrix slicing and factorization    | Reduced LUT usage by up to six times                     |
| Moroz et al. (2023)   | Mathematical Functions   | Piecewise linear exponential approximation | Low-complexity and fast FPGA-friendly implementations    |
| Paz et al. (2023)     | Arithmetic Units         | DSP-based complex multipliers              | High throughput with minimal DSP usage                   |
| Xing et al. (2023)    | Trigonometric Functions  | Recursive trigonometric technique          | Reduced storage and computation complexity               |
| Cho et al. (2021)     | CNN Acceleration         | Approximate accumulation units             | Reduced memory usage and network latency                 |
| Abd et al. (2021)     | Low-Power CNN            | Pruning and quantization                   | DSP-free CNN accelerator with high power efficiency      |
| Ahmad et al. (2021)   | Approximate Arithmetic   | Low-error approximate adders               | Reduced area and power with controlled error             |
| (Combined trend)      | FPGA-based AI Systems    | Approximation, quantization, parallelism   | Demonstrates FPGA suitability for edge and real-time AI  |

The research studies existing work on designing specific shallow neural network designs which help decrease FPGA resource consumption. Jiang et al. (2024) [64] developed a segmented spline curve neural network which includes adjustable activation functions to achieve deep-network-level precision with reduced resource requirements. Lehnert et al. (2023) [65] achieved significant LUT savings through their method which divides weight matrices into multiple parts while keeping all necessary computations. The researchers Pistellato et al. (2023) [66] and Nevarez et al. (2023) [67] studied quantization-aware training together with ultra-low-bit floating-point formats which showed high throughput and power efficiency while maintaining accuracy results near their original values.

**Figure 7: Application areas and optimization techniques used in FPGA-based studies**



The topic of CNN acceleration is still prevalent. Current applications of FPGA-based computational designs include linear and nonlinear spatial filters on real-time video content (Campos et al., 2024) [68] and approximate arithmetic, pruning, and DSP-free CNN accelerators to minimize latency and use of power number (Cho et al., 2021) [69] and Abd et al. (2021) [70]. The converged FPGA-based CNN accelerator framework suggested by Yang et al. (2023) [71] enhances the arithmetic performance and DSP usage in object detection operations to a greater extent. Moreover, a CNN inference scheme, where the use of multipliers is avoided and instead the lookup-table is performed, is presented in Fuketa et al. (2024) [72], which demonstrates comparable performance without the use of DSP blocks.

In addition to neural networks, FPGAs have been used on various high-performance areas. Tariq et al. (2024) [73] enhance the process of particle filtering by using parallel and pipelining of FPGA architectures. The optimization of cryptography pairing is applied to the server-side FPGAs by Sakamoto et al. (2024) [74], resulting in much higher throughput. The article of Hassan et al. (2023) [75] uses approximate calculating in a neural signal processing, which enhances in terms of speed and area efficiency. Senthilkumar et al. (2023) [76] present the implementation of biomedical signal analysis based on FPGA-based hybrid neural architectures, whereas Xing et al. (2023) [77] introduce a more efficient recursive trigonometric method that could be implemented on the FPGA.

### 5. *FPGA-Based Cryptographic and Secure Communication Systems*

The effectiveness of FPGA-based architectures in signal processing, control and sensing applications as well as in real-time, high performance and low power applications is well reported in the literature. Gaiceanu et al. (2025) [78] illustrate the use of FPGA-controlled harmonic reduction in power systems, whereas Garrido et al. (2020) [79] and Song et al. (2020) [80] note effective design of FFT and time-to-digital converters. Nada et al. (2024) [81] in fuzzy embedded control, Cuevas et al. (2022) [82] in low-power neural data compression and Won et al. (2021) [83] in PET/MR medical imaging explore the FPGA-enabled control and sensing systems further. Also, hyperspectral real-time target detection (Macias et al., 2022) [84] and space quality vision processing (Leon et al., 2021) [85] support the contexts of latency-demanding and resource-constrained applications in which FPGAs are well-suited.

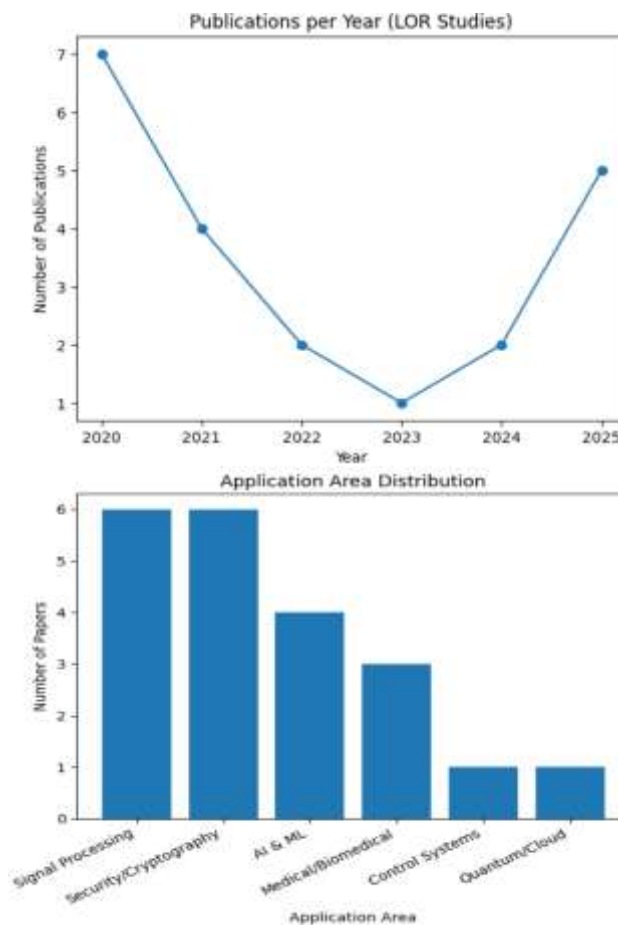
**Table 5: FPGA LOR-Based Cryptographic and Secure Communication Systems**

| <b>Authors (Year)</b>    | <b>Application Area</b> | <b>Method / Technology Used</b>      | <b>Key Contribution</b>                     | <b>Identified Gap / Limitation</b>        |
|--------------------------|-------------------------|--------------------------------------|---------------------------------------------|-------------------------------------------|
| Gaiceanu et al. (2025)   | Power systems           | FPGA-based APF control strategies    | Reduced harmonics and improved power factor | Limited discussion on scalability         |
| Wijesinghe et al. (2025) | Cryptography            | DSP-free FPGA modular exponentiation | Low-area, low-power crypto design           | Lower speed compared to DSP-based designs |
| Eamani et al. (2025)     | Image processing        | Approximate adders on FPGA           | Reduced power and LUT usage                 | Accuracy trade-off limits precision use   |
| Al-Hussein et al. (2025) | Image security          | Hyper-chaotic encryption on FPGA     | Strong image security implementation        | Increased system complexity               |
| Sugier et al. (2025)     | Cryptographic hashing   | DSP-based BLAKE3 on FPGA             | Power reduction using DSP blocks            | Limited benefit in pipelined designs      |
| Oukaira et al. (2025)    | Quantum computing       | FPGA & DSP-assisted quantum systems  | Comprehensive EQT review                    | Mostly theoretical analysis               |
| Shumran et al. (2024)    | Audio security          | Chaos-based audio encryption         | Detailed classification of methods          | No hardware implementation comparison     |

|                              |                       |                                   |                                 |                                      |
|------------------------------|-----------------------|-----------------------------------|---------------------------------|--------------------------------------|
| Nada et al. (2024)           | Control systems       | FPGA-based fuzzy logic control    | Fast parallel embedded control  | Limited real-world scalability tests |
| Stojilović et al. (2023)     | Cloud security        | FPGA attack and defense analysis  | Identified cloud FPGA threats   | No experimental mitigation framework |
| Cuevas et al. (2022)         | Biomedical signals    | FPGA-based data compression       | Reduced power and bandwidth     | Focused on specific neural signals   |
| Macias et al. (2022)         | Hyperspectral imaging | FPGA ATDCA-GS algorithm           | Real-time target detection      | Algorithm-specific implementation    |
| Won et al. (2021)            | Medical imaging       | FPGA-only PET/MR DAQ              | High-resolution brain imaging   | Complex hardware setup               |
| Papathéofanous et al. (2021) | 5G communication      | FPGA LDPC accelerator             | High-throughput decoding        | Encoding less efficient              |
| Leon et al. (2021)           | Space applications    | Radiation-hardened FPGA           | Reliable space-grade processing | Limited frame rate                   |
| Garrido et al. (2020)        | Signal processing     | Constant multiplier FFT           | Reduced DSP and BRAM usage      | Design complexity increases          |
| You et al. (2020)            | AI acceleration       | Sparse CNN FPGA accelerator       | Improved DSP efficiency         | Requires pruning optimization        |
| Conti et al. (2020)          | Video systems         | FPGA SDI verification framework   | Cost-effective testing          | Limited to SDI protocols             |
| Hebibi et al. (2020)         | Communication systems | FPGA-based BPSK modulation        | Simple low-cost implementation  | Limited modulation schemes           |
| Song et al. (2020)           | Measurement systems   | Temperature-compensated TDC       | High timing accuracy            | Additional LUT overhead              |
| Kawashima et al. (2020)      | Neural computing      | Chaotic Boltzmann machine on FPGA | Massive speed improvement       | Fixed-point precision limits         |
| Nomani et al. (2020)         | ISR systems           | Approximate computing on FPGA     | Improved SWaP performance       | Accuracy control required            |

Quite a significant part of the research is devoted to the security, cryptography and chaotic systems that are executed on FPGAs. Wijesinghe et al. (2025) [86] and Sugier et al. (2025) [87] provide efficient cryptographic hardware designs of modular exponentiation and hash implementation of the low-power BLAKE, respectively. For image encryption, Al-Hussein et al. (2025) use chaos-based encryption methods to ensure multimedia security [88] when Shumran et al. (2024) use these methods to provide audio encryption systems [89]. Stojilović et al. (2023) [90] focus on security issues in shared and cloud-based FPGA platforms and Oukaira et al. (2025) [91] argue about the role of FPGA and DSP systems in future quantum calculating and secure communication systems. These works all highlight the fact that FPGA is able to provide secure hardware-level protection with higher performance.

**Figure 8: Publications per Year and Application Area Distribution**



Accurate computing and AI acceleration, as well as novel paradigms on FPGA platforms are also noted in recent studies. Designs for approximate arithmetic suggested by Eamani et al. (2025) [92] and Nomani et al. (2020) [93] prove to be far more efficient in power consumption in addition to speed in processing of images and videos. You et al. (2020 [94]) and Kawashima et al. (2020) [95] use sparse CNN accelerator and chaotic Boltzmann machine, respectively, to accelerate AI and neural models on FPGA. Papatheofanous et al. (2021) [96] investigate 5G Open RAN LDPC acceleration communication and verification structures, and Conti et al. (2020) [97] investigate SDI

video protocol testing, whereas Hebibi et al. (2020) [98] investigate FPGA-based modulation systems. These studies also indicate that there is a favored hunting direction towards resource conscious and scaleable and application-focused FPGA solutions and also the future prospects of power streamlining, security-assimilation and intelligent hardware-design.

## **6. *FPGA-Based FIR Filter Architectures and Performance Optimization in Digital Signal Processing***

Maamoun et al. (2021) [99] emphasized that the poor performance of processor based implementation of DSP algorithms is frequently caused by architectural trade-offs made on behalf of programmability and thus replacement by FPGA based realizations in which architecture can be designed to trade-off performance. Their analysis showed that the current FPGAs, which have specialized DSP macro blocks, are much more efficient in FIR filter implementations especially direct and transposed filter structures on platforms like Xilinx Spartan-6. Based on the FPGA-based DSP studies, Arucu et al., (2025) [100] investigated the research on FIR filter design and implementation, resource utilization, silicon area and real-time performance of FIR filters through MATLAB-assisted synthesis and comparison between the HDL-generated filters and vendor-supplied Soft-IP cores. Their results underlined the need to have design methodology to balance performance and hardware efficiency. To overcome the complexity of hardware, Venkateswarlu et al. (2018) [101] offered a low-cost Radix-4 reconfigurable FIR (LC-R4-RFIR) filter architecture, which reduced the use of LUTs, space, and power consumption through an effective multiplication strategy, and demonstrated high performance on various Xilinx Virtex machines. In more current work, Fata et al. (2025) [102] made the move away from computation and instead focused on data movement with a memory-aware FPGA optimization framework that by rearranging memory access patterns and buffering strategies achieved significant improvements in reducing latency, increasing throughput, and lowering power consumption. Taken together, these studies indicate that to satisfy the current real-time processing requirements, high-performance FPGA-based DSP systems should not only be designed in an optimized way with respect to computational architecture, but also be designed with an efficient memory layout and resource-aware design approach.

## **7. *Discussion***

The reviewed literature shows that FPGA-based digital signal processing experienced substantial growth from 2020 to 2025 because engineers required computing systems that delivered high-speed processing with minimal delays while using low energy consumption. The discussion explains how FPGA architectures function as a complete solution between algorithm development and its actual operation on physical hardware by using their ability to process multiple tasks simultaneously through pipelined execution and system reconfiguration [99-102]. The DSP systems that use FPGA technology demonstrate superior performance in both reliability and processing capacity when compared to standard processing systems which makes them ideal for use in communication systems and biomedical signal processing and radar operations and new AI-based applications. The implementation of advanced design methods which include high-level synthesis and hardware-software co-design has simplified development tasks while enabling designers to achieve greater productivity. Another key takeaway is that more and more studies are focusing on optimization techniques like precision tuning, quantization-aware design, and reduced-precision arithmetic to find a sweet spot between accuracy and resource efficiency in real-time

and power-constrained scenarios. The papers reviewed show a clear tendency toward heterogeneous and application-specific architectures, where FPGAs combine embedded processors and accelerators for better flexibility and scalability. However, there are still challenges in finding the best balance between performance, power consumption, and numerical accuracy. In general terms, this discussion validates FPGA-based DSP as an effective and flexible approach while pointing out the need for standardized evaluation metrics and scalable design frameworks in future research.

### **8. Conclusion**

This review of the literature finds that FPGA-based digital signal processing has emerged as a platform to provide high-performance, real-time, and energy-efficient computing in a wide range of application areas. The proposed systematic review is a PRISMA-based systematic review that gives a structured and open evaluation of the latest developments in FPGA-based digital signal processing in 2020-2025. Through the PRISMA, the study had a strict procedure of identifying, screening, eligibility, and including of relevant literature. In the first step, 1970 records were identified using the SCOPUS database, and the records that were identified were then subjected to stringent inclusion and exclusion criteria, which helped in the selection of 51 high quality journal articles which were to be analysed finally. The implementation of modern design practices, such as high-level synthesis, model-based design, and hardware-software co-design has enabled the development process to become much easier without compromising portability and productivity. Pipelining, parallel architectures, precision tuning, and quantization-conscious design are some of the essential optimization techniques that help to strike positive trade-offs among the accuracy, latency, and power as well as the use of hardware resources. Moreover, their versatility and relevance in the future are emphasized by the increased use of FPGAs in artificial intelligence, communication, biomedical, and secure processing. There are still scalability, standardized benchmarking and handling of precision performance trade-offs issues with heterogeneous systems despite these advances. On the whole, this review confirms that FPGA-based DSP platforms have a great potential in signal-processing systems of the next generation and are open to valuable research in adaptive processors, smart optimization models and energy-aware design specifications.

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