# *EFFICIENT ARCHITECTURE OF COMBINED RADIX DIF ALGORITHM FOR MIMO-OFDM APPLICATION*

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***Abstract:*** An efficient design of combined radix-2 Single path Delay Feedback (SDF)-Single path Delay Commutator (SDC)-Decimation In Frequency (DIF) algorithm is proposed in this paper which can be used in Orthogonal Frequency Division Multiplexing (OFDM) with Multiple Input Multiple Output (MIMO) applications. The MIMO-OFDM communication system has tremendous and swift growth in various applications used over last decade, especially wireless and digital communication where adaptability, reconfigurability, less chip size, hardware improvements, and lower power consumption are mandatory requirements during communication. The main aim of this structure is to improve the performance of combined Fast Fourier Transform (FFT) for the MIMO-OFDM system and also to reduce the complexity of the hardware.

***Keywords:*** MIMO-OFDM System, Decimation in Frequency, FFT.

## *I. INTRODUCTION*

In recent years, FFT has played a significant role in MIMO-OFDM communication system applications. In many advanced communication systems such as wireless networks, ultra wide band (UWB), digital video broadcasting (DVB), and digital audio broadcasting (DAB), MIMO-OFDM is used. The FFT calculation must be high-throughput and low-latency in all these systems. Therefore, high-performance FFT circuit design is an efficient solution to the above-mentioned issues.

MIMO-OFDM techniques face a lot of challenges in the present world. For improving their architecture investigation, different FFT model has been designed by large endeavours. The several types of sources such as digital bits, voices, videos, broad broadcast messaging, command and control signals are assumed to analyze the data transmission properties of the MIMO-OFDM system. FFT brings cost efficiency, flexibility, and power to drive and establish long distance communications.

In this paper, pipelined combined radix DIF architecture is designed. The combined DIF FFT architecture is used to increase the throughput and speed of the processing element. To improve the performance of architecture, combined FFT structure is proposed. In this work, to reduce the power, area and latency in terms of Very Large Scale Integration (VLSI) concerns.

## *II. LITERATURE SURVEY*

The fourth generation mobile communication system (4G) uses adaptive OFDM. Because adaptive OFDM system uses adaptive modulation/demodulation

technique, it transfers the data in higher order and higher transmission rate than compared to conventional OFDM system [1]. Adaptive modulation scheme decreases the channel fading and increases the throughput of the system. Generally, OFDM is a multicarrier modulation technique in which a large number of orthogonal subcarriers is used. FFT is used to generate the signal in the OFDM [2].

Individual carrier known as sub carrier is modulated at low symbol rate in the conventional OFDM. In an adaptive OFDM system data is generated by using data generator. Here the data is represented by a code word. Before transmitting the data in the channel, first, it converts the data from serial to parallel [3]. The channel information is sent to the transmitter before transmitting the signal. An inverse FFT (IFFT) is used for the conversion of the signal from frequency domain to time domain. It is useful for OFDM system to maintain the orthogonality between the subcarriers [4].

In a VLSI based FFT and IFFT are the two important processes in many communication systems [5]. Two methods are used to implement the FFT and IFFT process in VLSI. They are parallel process and pipelined process. Most of the communication system uses the pipelined processor for speed and efficient data transmission. Before going to implement the designer remember to design the pipelined processor with lower memory requirement [6]. The pipelined architecture contains different methods named as single delay path feedback, single delay path commutator, multi path delay feedback, and multipath delay Commutator [7]. Depends on the type, the requirement of the process is also changed. The main motive of the FFT process is to minimize the memory requirement in the pipelined FFT, and also consider the power consumption, latency, and complexity of the processor [8].

## *III. PROPOSED COMBINED RADIX DIF FFT*

In this paper, the proposed combined radix-2 SDF-SDC DIF-FFT architecture for the MIMO-OFDM communication system is designed. Radix 2 SDF-SDC have various advantages in terms of VLSI factors like less area utilization, high speed and low power consumption. The combined SDF-SDC architecture has less computational path and also improve the performances of FFT processor. Proposed combined SDF-SDC architecture is used to perform a single stage of single-path delay feedback, and all other stages are used in SDC. Figure 1 shows the combined radix-2 DIF-FFT architecture.

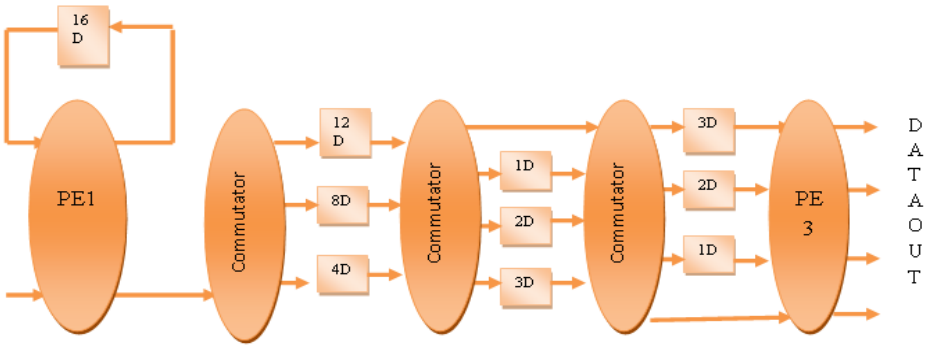


***Fig. 1 Proposed Combined Radix DIF FFT***

## *IV. RESULTS AND DISCUSSION*

The Verilog Hardware Description Language (Verilog HDL) is used to design the proposed combined radix-2 SDF-SDC DIF FFT architecture. The combined architecture is simulated and synthesized using ModelSim 6.3C and synthesized using Xilinx 12.4i Plan-ahead tool respectively. Figures 2 and 3 show the synthesis result of combined radix FFT for area consumption and delay consumption respectively. Table 1 shows the performance of combined radix FFT with existing algorithm.

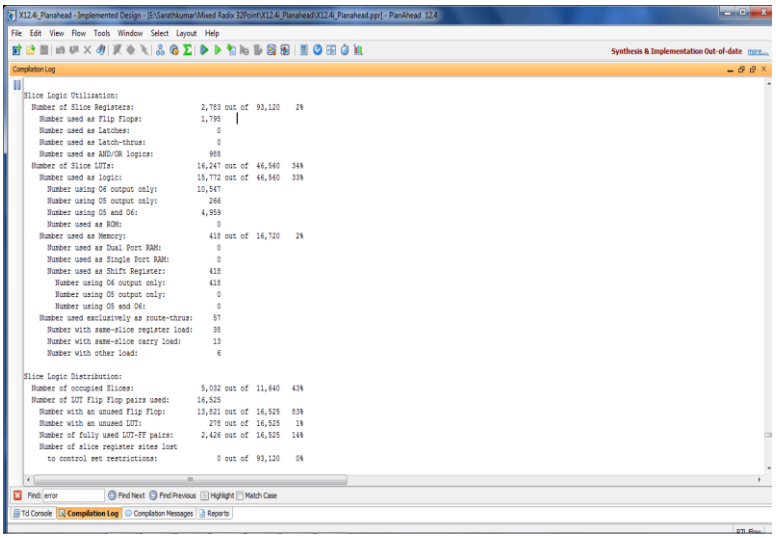


***Fig. 2 Synthesis Result of Combined Radix FFT for area consumption***

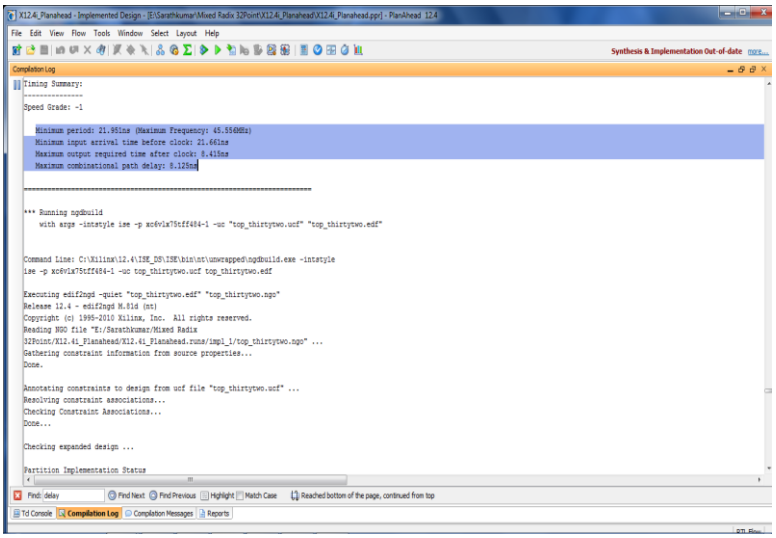


***Fig. 3 Synthesis Result of Combined Radix FFT for Delay consumption***

***TABLE 1 Comparison analysis of Existing and proposed method***

| Type | Number of occupied Slices | Number of LUTs | Delay(ns) |
|---|---|---|---|
| Existing method | 9523 | 21,331 | 15.213 |
| Proposed method | 5032 | 16,247 | 8.415 |

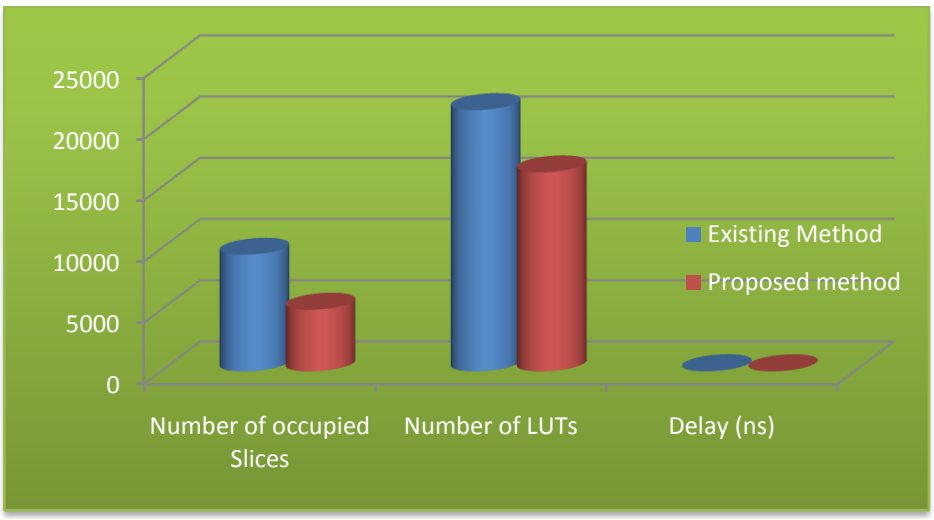


***Fig. 4 Performance Evaluation of existing and proposed combined radix DIF algorithm***

## *V. CONCLUSION*

In this paper, the architecture of combined radix-2 SDF-SDC DIF FFT architecture is designed through VLSI design environment. Combined radix FFT architecture is to increase the speed of processing element. This system reduces the computational path of frequency transformation techniques. The proposed method offers 47.1% and 44.6% reduction in area and delay than the existing method. In future, the proposed combined radix DIF-FFT and it will be integrated into MIMO-OFDM communication application for improving the process of data communication.

## *REFERENCES*

[1]. V. Arunachalam, and A.N.J. Raj, "Efficient VLSI Implementation of FFT for Orthogonal Frequency Division Multiplexing Applications", IET Circuits, Devices and Systems, Vol. 8, No. 6, 2014, pp. 526-531.

[2]. M. Ayinala, and K.K. Parhi, "FFT Architectures for Real-Valued Signals Based on Radix-$2^3$ and Radix-$2^4$ Algorithms", IEEE Transactions on Circuits and Systems, Vol. 60, No. 9, 2013, pp. 2422-2430.

[3]. J. Chen, J. Hu, S. Lee, and G.E. Sobelman, "Hardware Efficient Mixed Radix-25/16/9 FFT for LTE Systems", IEEE Transactions on Very Large Scale Integration Systems, Vol. 23, No. 2, 2015, pp. 221-229.

[4]. A. Kaivani, and S.B. Ko, "Area Efficient Floating Point FFT Butterfly Architectures Based on Multi-operand adders", Electronics Letters, Vol. 51, No.12, 2015, pp. 895-897.

[5]. H.F. Luo, Y.J. Liu, and M.D. Shieh, "Efficient Memory-Addressing Algorithms for FFT Processor Design", IEEE Transactions on Very Large Scale Integration Systems, Vol. 23, No. 10, 2015, pp. 2162-2171.

[6]. S. Qiao, Y. Hei, B. Wu, and Y. Zhou, "An Area and Power Efficient FFT processor for UWB Systems", IEEE, 2007, pp. 582-585.

[7]. V. Arunachalam, and A.N.J. Raj, "Efficient VLSI implementation of FFT for orthogonal frequency division multiplexing applications" IET Circuits, Devices & Systems, Vol. 8, No. 6, 2014, pp.526-531.

[8]. A. Akshata, D.K. Gopika, and I.Hameem Shanavas, "FPGA Implementation of Decimation in Time FFT or Discrete Fourier Transform", JEST-M, Vol. 1, No. 2, 2012, pp. 35-39.